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Leakage Immune 9T-SRAM Cell in Sub-threshold Region

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Abstract

The paper presents a variability-aware modified 9T SRAM cell. In comparison to 6T SRAM cell the proposed cell achieves 1.3× higher read-SNM and 1.77× higher write-SNM with 79.6% SINM (static current noise margin) distribution at the expense of 14.7× lower WTI (write trip current) at 0.4 V power supply voltage, while maintaining similar stability in hold mode. Thus, comparative analysis exhibits that the proposed design has a significant improvement, thereby achieving high cell stability at 45nm technology.

Keywords*: Low power SRAM; Process variations; Sub-threshold SRAM; Static noise margin; Stability*

1. Introduction

SRAM (static random access memory) cell stability with voltage scaling is a primary concern in deep sub-micron technology [1]. As SRAM is scaled with lower supply voltage and technology, sufficient static noise margin (SNM) becomes difficult to maintain in the conventional 6T (C6T) SRAM cell. The common approach to meet the stable operation in sub-threshold regime is to add more transistors to the C6T cell and these are widely deemed to be inevitable in order to support future process technologies. In paper [2], the design and evaluation of nine transistors (9T) has been done which utilizes a scheme with separate read and write word lines. The result shows improvements in power dissipation, performance and stability. In paper [3], a high density 8T-SRAM cell has been designed to achieve a minimum operating voltage of 350 mV at 65nm technology. To ensure read stability, buffered read technique is used, and peripheral control of both the bit-cell supply voltage and the read-buffer's foot voltage enable sub- write and read without degrading the bit-cell density. An overall result shows that the entire 256 kb SRAM consumes 2.2 W in leakage power at 350mV. In paper [4], a new nine-transistor (9T) SRAM cell has been designed at 65nm technology for reducing leakage power and enhancing data stability. This cell completely isolates the data from the bit lines during a read operation, leakage power consumption of a super cutoff 9T SRAM cell was reduced by 22.9% as compared to a conventional six-transistor SRAM cell. Hence, the cell structures with more transistors are widely deemed to be inevitable in order to support future process technologies as well as in sub-threshold region of operation. A sub-threshold operating voltage leave less room for large SNM and provides inaccurate logic cells characterization, sensitive performance, instable functionality due to process, voltage, and temperature (PVT) variations and read/write stability problems. This paper proposes a modified nine transistors SRAM cell (hereafter called M9T) and their thorough evaluation performance which is compared with 6T in sub-threshold regime at 45nm technology. The rest of the paper is organized as follows. Section 2 presents the detailed analysis of proposed M9T and read/write current operation. Sections 3 present the overall current analysis of proposed M9T for read and write operation. Section 4 describes the simulation methodology and result discussion. Section 5 presents a summary of the paper and concluding remarks.

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2. Design of Proposed M9T

The schematic of proposed M9T is shown in Figure 1. This design is the modified version of TG-based fully differential 8T SRAM bit cell [5]. The internal architecture of this cell consists of cross-coupled inverter pair (MP1/MN1) and (MP2/MN2) to store 1-bit information inside the cell. The access transistors are replaced with transmission gate pairs (MN3/MP3 and MN4/MP4) and are controlled by an extra added PMOS transistor (MP5). The gate terminal of the MP5 is connected to WL of the cell. The transmission gates based access transistors used to communicate one-bit information with the outside of the cell. As long as the transmission gate based access transistors are turned off via a WL, the cell keeps one of its two possible steady states either logic '0 or logic '1. During the read and write operations, common WL controls accessibility to the cell nodes Q and QB through these access transistors. The additional PMOS transistors is connected in such a way that no additional control lines would be needed to switch the data of the cell, it helps to overcome the voltage degradation and balance the leakage currents of the access transistors observed at 45nm technology.

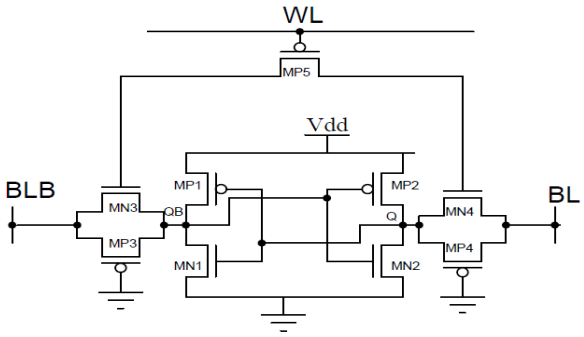

Figure 1. Design of M9T

2.1. Read Operation of M9T

Circuit set up for read operation of M9T is shown in Figure 2. Assuming that logic '0' is stored in the cell. The transistors MP2 and MN1 are turned off, while the transistors MP1 and MN2 operate in linear mode. Thus internal node voltages are Q = '0' and QB = '1' before the transmission gate based access transistors (MN3/MP3 and MN4MP4) are turned on. During read operation, the bit-lines (BL/BLB) are pre-charged to a high level (V_{DD}) and word-line (WL) is enabled (pulsed to a low level) which turns-on the extra added PMOS transistors (MP5). After the transmission gate based access transistor pairs (MN3/MP3 and MN4/MP4) are switched on, the voltage at BLB will not have a significant variation as no current flows through MP3 and MN3 due to BLB & QB =1 at both end. On the other hand MN4/MP4 and MN2 will conduct and the voltage level of BL line will begin to drop slightly, so that a differential voltage develops between the bit-lines which are sensed by sense amplifier. The read operation would be stable provided the node voltage Q does not exceed the threshold voltage of MN1.

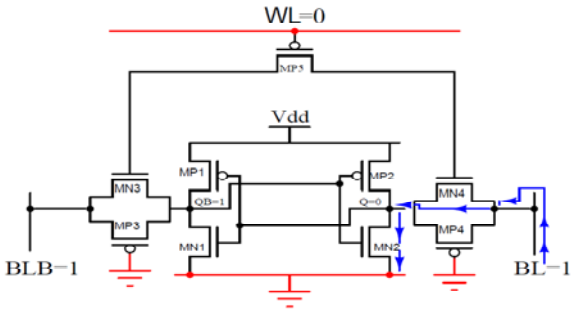

Figure 2. Test circuit for read operation of M9T

2.2. Write Operation of M9T

Circuit set up for write operation of M9T is shown in Figure 3. Consider a write '0'operation, assuming logic'1' is stored in the SRAM cell initially. The transistors MP1 and MN2 are turned off, while the transistors MN1 and MP2 operate in linear mode. Thus internal node voltages are Q = '1' and QB = '0' before the transmission gate based access transistor pairs (MN3/MP3 and Mn4/MP4) are turned on. During write operation, the bit-lines BLB is pre-charged to a high level (VDD) and BL is pre-charged to low level (logic '0') and WL is enabled (pulsed to a low level) which turns on the extra adder PMOS transistor (MP5) as well as the corresponding transmission gate based access transistor pairs. After the transmission gate based access transistors MN3/MP3 and MN4/MP4 are switched on, the voltage at node QB should not rise above the threshold voltage of MN2 to change the stored information i.e. forcing node Q ='0' and QB ='1'. For successful write operation the node voltage Q should be reduced below the threshold voltage of MN1. For stable write and read operation the aspect ratios of the transistors (MP4, MN2) and (MP3, MN1) have to be computed accurately.

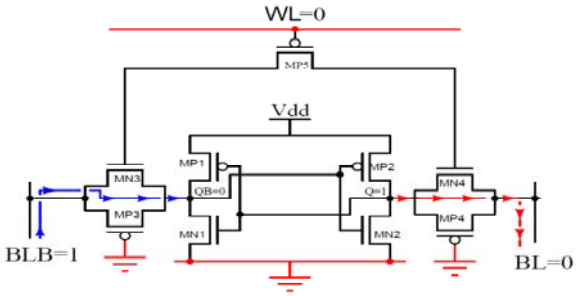

Figure 3. Test circuit for write operation of M9T

3. Current Analysis of Proposed M9T

Figure 4 shows direction of the read and write current flow through the proposed M9T. At the start of a read operation, the bit line pair (BL/BLB) is pre-charged to high voltage (V_{DD}) and then word line (WL) is asserted to low voltage, which enables MP3 as well as transmission gate based access transistor pairs (MN3/MP3) and (MN4/MP4). As a result, cell current or read current (I_{read}) begins to flow from BLB goes in through MP3/MN3 to MP1 and flows out through MN2 to GND.

I_{read} can be expressed analytically by solving Kirchhoff's current law at internal node 'Q' storing '0'

I_{read} = *FUNCTION* (I_{MN3}, I_{MP3}, I_{MP1}, I_{MN2})

Where BLB & BL = '1', WL = '0', QB= '1' and Q= '0'

$$I_{read} = I_{MN3+I_{MP3}} + I_{MP1} - I_{MN2} \quad (1)$$

The amount of read current flowing through the cell directly determines how fast the bit lines can be discharged. The magnitude of the read current therefore significantly influences the maximum speed of the memory.

During write operation, one of the bit lines is pre-charged to high voltage (V_{DD}) and maintains the other at GND. Thereafter, WL is asserted, which enables MN5 and MN6. As a result, write current (I_{write}) begins to flow from BL goes in through MP2 to MN6 and flows out through MN1 to GND.

I_{write} can also be expressed analytically by solving Kirchhoff's current law at internal node ''Q'' storing ''1''

I_{write} = *FUNCTION* (I_{MN4}, I_{MP4}, I_{MP2}, I_{MN1})

Where BLB = '1', BL = '0', WL = '0' (ON), Q= '1' and QB= '0'

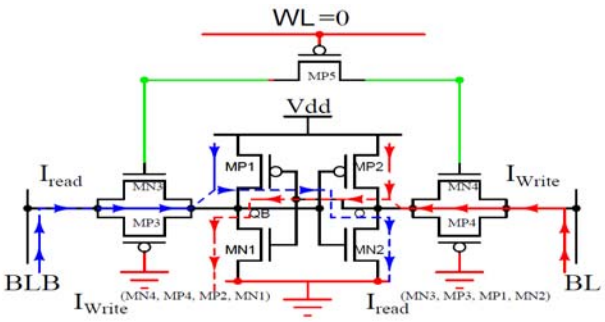

Figure 4. Read and write current flow through M9T

$$I_{write} = I_{MN6} + I_{MP2} - I_{MN1} \quad (2)$$

Stronger pass gates and slightly weaker pull up transistors are normally employed to ensure a robust write operation in the worst case process corner.

4. Simulation Results and Discussions

This section presents comparative analysis of various design metrics like read-stability, write-ability, hold stability, SINM and WTI of the proposed M9T and C6T. These design metrics are estimated with Monte Carlo simulation using 45nm technology in sub-threshold regime.

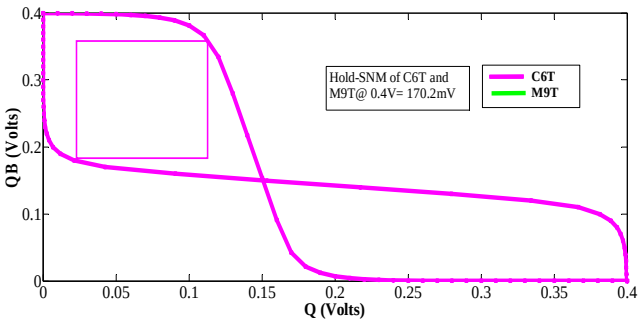

Figure 5. VTC's of M9T and C6T during HOLD operation

4.1. Hold Operation of M9T

The primary metric in nano-scale SRAM design is stability which is analyzed by computing SNM in hold mode. This hold SNM metric, first defined by Seevinck et al. [6], measures the maximum serial dc voltage that can be applied to the internal nodes of the cell without flipping the state of the cell or minimum dc noise voltage required to flip the state of the cell.

The side length of the largest square that can be embedded inside the lobes of the butterfly curve represents the hold SNM of the cell. Figure 5 shows "butterfly curve" or VTC's of M9T and C6T, during HOLD operation by varying supply voltage from 0.2 to 0.4V respectively. The two curves are merged into each other as expected since cross coupled inverter pair designs are similar for both [7].

4.2. Read Operation of M9T

Read stability, analyzed by RSNM, is an important design metric of SRAM cell. Measurements of RSNM is carried out in a similar fashion as done for hold SNM with BL/BLB pre-charged to V_{DD} and WL is biased in ON state with, logic '1' (discussed in Section 2). The cell ratio (CR) defined as CR = β_{driver} /β_{access} gives an idea about how much high the node storing '0' rises during read operation. During read access, CR is critical for value of the logic '0' at Q. The lower value of CR requires smaller noise voltage at Q to trip the cell, thereby compromising on speed and read-stability. The higher values of CR provide higher I_{read} and improved stability at the cost of increased cell area. Figure 6 represents RSNM "butterfly curve" for both (S8T and C6T) cell. The M9T has 1.3× higher RSNM compared to the C6T for CR= 1.5, (at V_{DD} =0.4 V).

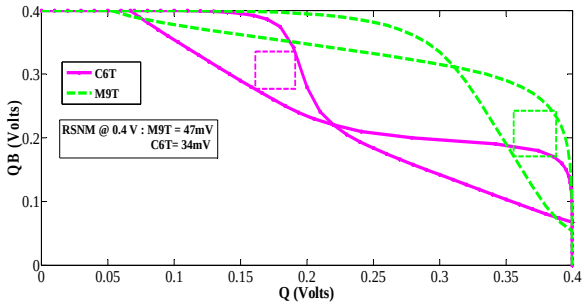

Figure 6. VTC's of M9T and C6T during read operation

4.3. Write Operation of M9T

Write stability, analyzed by write-SNM (WSNM), is the minimum voltage necessary to drive the bit cell into a mono-stable state during a write operation. Measurements of WSNM is carried out when one of the BL/BLB line is pre-charged to high voltage (V_{DD}) and WL of the cell is biased at active mode, logic '1' '(discussed in Section 2). During write operation, the bit-line pair directly connects to the node Q and QB and forces the nodes Q and QB (the stored information) to obtain required voltage levels. On completion of change in state, WL signal is asserted low, and cross coupled inverter pair stores the written 1-bit information. The write-ability of the cell depends on the pull up ratio (PR) defined as PR = β_{pullup} /β_{access}. A high value of PR is critical for storing logic "1" at Q to ensure a robust write operation in the worst case process corner. Figure 7 represents the VTC curve for WSNM of C6T and S8T.

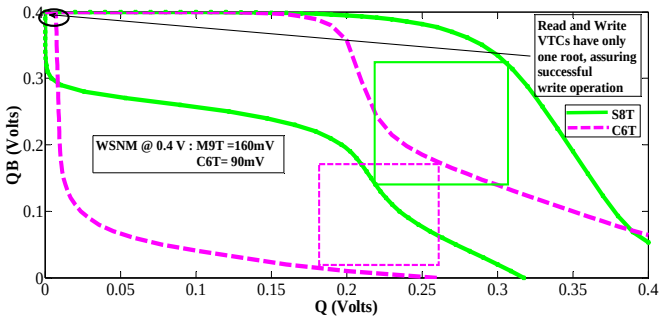

Figure 7. VTC's of M9T and C6T during write operation

As observed from Figure 7, there is only one intersection point of both the VTC's curve. This indicates the single stable point which signifies the successful write operation and functionality of the cross coupled inverters of the cell as mono-stable circuit. The M9T and C6T show 160 mV and 90 mV WSNM respectively giving 1.77 × improvements.

4.4. Alternative Noise Margins

An alternative noise margin method based on N-curve metrics (NCM) of the cell [8] is used for the evaluation of robustness of the SRAM cell, Figure 8 shows the test circuit for extracting NCM of M9T during read mode. Bit-line pair is pre-charged to V_{DD} and WL is pre-charged at logic "1" (ON state) for the NCM analysis [9]. An external voltage source (V_{IN}) is applied at the input storage node "QB". V_{IN} is swept from 0 V to V_{DD} and corresponding input current (I_{IN}) produces the NCM characteristics as shown in Figure 9. Basically three common metrics known as static voltage noise margin (SVNM), SINM and WTI are found in the NCM of the cell. The curve is analyzed at the three points (A, B (B1) and C), where it crosses zero. Point A and C are the two stable points, while B (B1) is a meta-stable point. The voltage difference between A and B gives SVNM which indicates the maximum tolerable dc noise voltage at the internal node "QB". The analyzed results of NCM give SVNM value of 210 mV for M9T and 220mV for C6T. The positive peak current between A and B indicates the stability of the cell, characterized as SINM which indicates the maximum injected dc current in the SRAM cell required to flip the content. The analyzed results of NCM give 49.1µA and 10µA of SINM for M9T and C6T respectively.

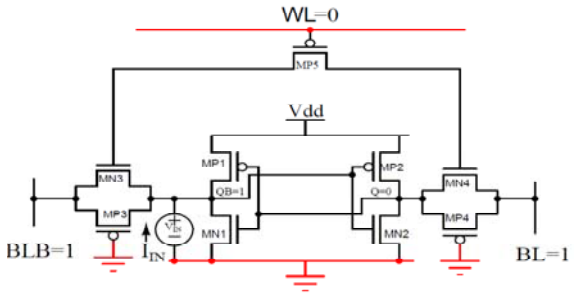

Figure 8. Test circuit for extracting N-curve of M9T during read

The third metric WTI is the amount of current needed to write the cell when both bit-lines are kept at V_{DD}. The negative current peak between point B and C gives WTI. Figure 18 shows -58.9 µA and -4µA WTI for M9T and C6T respectively. For better read and write stability of the design, it is preferable to have smaller value of WTI and larger value for SINM. The S8T bit cell gives significant improvement in terms of SVNM, WTI, SINM and WTV.

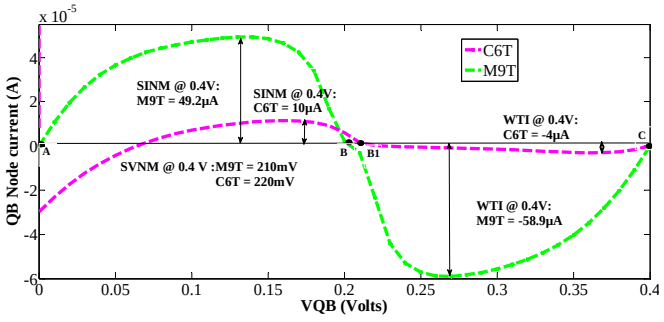

Figure 9. Combine N-curve of M9T and C6T during read mode

5. Conclusion

Acute problem of variability is found in standard CMOS technology due to technology scaling driven by benefit of integration density, lower power dissipation and overall power delay product. This work proposes a robust, high noise tolerant differential 9T SRAM cell at 45 nm technology in sub-threshold regime. The thorough analyses on various parameters like read current, access delay, read stability, hold power etc. are presented. The M9T exhibits 1.3×

higher read-SNM and 1.77× higher write-SNM indicating robustness of operation at 0.4V power supply voltage as compare to C6T. This is achieved without inserting an additional control line to switch the data into the M9T. The proposed design is an attractive choice for low power based application in scaled technology.

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