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Review on Fin Shape Channel Field Effect Transistor (FinFET)

Yasir H. Naif
Department of Computer Engineering, Tishk International University (TIU), Erbil, Iraq

Corresponding author: Yasir Hashim (e-mail: yasir.hashim@ieee.org).

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ABSTRACT Moore's law principle of minimization of transistors indicates that the number of transistors in integrated circuit (IC) doubles about every two years, but the down scaling of MOSFET towards nano dimensions tends to short channel effects problems, especially the lower ON to OFF current ratio and increasing the DIBL. This happen because of the nano-traditional structure of MOSFET has a high depth to length ratio of transistors channel and this leads to increase the OFF current. The method of this research includes a review of FinFET structure as a new MOSFET structure to overcome the short channel effects especially the ON to OFF current ratio and DIBL. As a final conclusion and result of this study, the FinFET structure has better characteristics in nano dimensions with excellent ON to OFF current ratio, subthreshold swing and DIBL.

INDEX TERMS FinFET, MOSFET, I_{on}/I_{off}, DIBL.

I. INTRODUCTION

Electronic engineering has played an important role in the development of science and knowledge and, most importantly, in the Evolution of integrated circuit manufacturing (ICs) [1-3], this happened as a result of the revolution in the minimization of transistors, the basic unit of the IC chips [4, 5], which have emerged in the size of tens of nanometres [6, 7]. According to the Moore's Law, in the ICs, the number of transistors is quadruple with doubling the performance in every three years (**FIGURE 1**), The major progress has been accomplished through minimizing the MOSFETs from larger dimensions of transistor to smaller transistor in nano-dimensions, results to increased density and speed [8, 9]. As continuous operation to shrink in the drive toward higher circuit density, but the reverse consequences happen from short channel effects (SCE) and become highly significant [10-12].

Following the Moore's prophecy, Dennard's Scaling law states that the transistors become faster, consume less power, and are cheaper to manufacture as they shrink. Thus, the Operational characteristics of a transistor can be preserved and the performance is improved if the critical parameters are scaled down by a factor, the critical parameters are as following: Device dimensions, Device voltages, Doping densities.

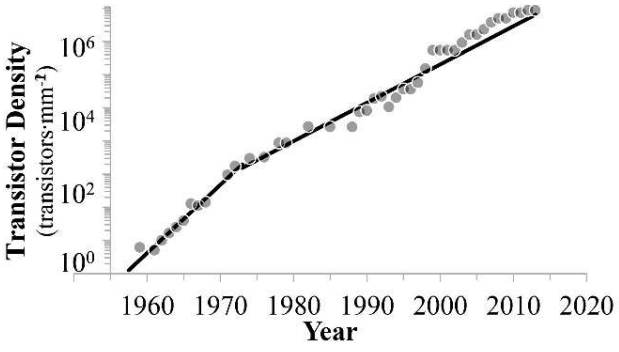


FIGURE 1. Yearly increased of Transistor density according to Moore's Law [8].

It is also known as the constant field scaling as both power supply and device dimensions' scale down. Power dissipation is becoming a major concern with the current

market scenarios. With the current scaling trend, power dissipation for every transistor reduces by a factor of two keeping the frequency constant. In order to support the power scaling, the power supply should be reduced. However, with the V_{dd} scaling, threshold voltage (V_{th}) should also scale simultaneously to maintain the drive current. However, V_{th} does not follow the scaling trend as expected. Power dissipation has increased drastically until the early 2000's due to frequency increase with considerable pipelining.

Significant progress has been achieved by reducing MOSFETs from Micro to Nano-dimensions transistor, resulting in increased speed and density Some constraints have led to the prediction of the end of technological advances in the semiconductor industry. The conventional MOSFET reduction beyond the 50 nm channel length has resulted in innovations to circumvent the barriers due to basic physics that restricts the traditional MOSFET. Limitations on the reduction of low-impedance-resistance circuits [13, 14] are as follows:

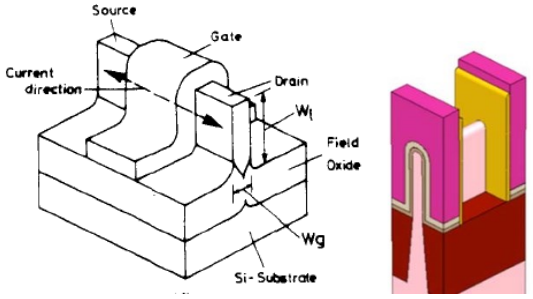
a. Increase the leakage of the current gate due to the quantum mechanical tunnel of the tankers through the thin gate oxide.
b. I_{OFF} increase due to the quantum mechanical tunnel of the tankers from exchange to the body, and from the source to the MOSFET drain.
c. Lower I_{on}/I_{off} ratio because of the lower control of the density and location of dopant atoms in the MOSFET channel and source/drain region to provide a high on to off current ratio.
d. Lowering of subthreshold slope.

There has been a significant deterioration in the performance of the interferometric wavelength converters (IWCs) in recent years because of their unstable hierarchy. One of the important parameters in the MOSFETs is the Subthreshold Slope (SS), which is defined as the change in the voltage of the gate (Vg) required to change the magnitude of current from OFF to ON state. The SS of a MOSFET is governed by thermionic emission-carrier diffusion over a thermal barrier and limited to 60 mV/decade at room temperature [15]. Thus, the further minimization of MOSFET is very difficult without a significant increase in I_{OFF}. For future IC based consumers, super low energy and energy efficient transistors with SS are needed with acceptable [15].

II. FinFET as a Nano-Transistors

The rapid development of integrated circuit technology has led to continuous reduction of transistors, resulting in continuous improvements in transistor performance. However, new studies have indicated that the lengths of the gate transistor to levels below 22 nm can result in many serious problems, such as high sub-threshold leaks, short channel effects, and device changes from one device to another. Thus, many researchers have attempted to overcome these problems by designing new transistor structures, such as the FinFET field effect transistor, and silicon nanowires. Field effect transistors (SiNWT). FinFET is a modified Nano version of MOSFET, illustrated by the FinFET structure in **FIGURE 1**. The researchers focused on the invention of new MOSFET structures after overcoming the MOSFET restrictions.

FinFETs are relatively easy to manufacture and have no alignment design problems affecting many other transistors [16]. Fin field-effect transistor (FinFET) is an advancement based on a device called fully depleted lean channel transistor DELTA [17], which was described in a scholastic publication in 1989. Both the design of DELTA and FinFET devices, shown in **FIGURE 2 (a),** share the same concept: the channel of the device is very thin compared with the large source and drain junctions. Because both sides of the channel are wrapped by the gate dielectric and the gate, the control of the gate over the channel is remarkably better than that of the planar MOSFET. This is the reason why the leakage current of FinFETs is far smaller than that of planar MOSFETs. The inversion layers' form at both sides of the channel so the device channel width can be approximated as twice of the fin height. The drive current of the FinFET can be easily multiplied by designing several fins in one FinFET device as in **FIGURE 2 (b)**, [18].



(a) (b)

FIGURE 2. Cross-sectional schematics of (a) DELTA transistor [17] (b)FinFET transistor [18].

Although the FinFET has more advantages in device performance than planar MOSFET, the momentum for FinFET development in academia did not pick up until early 2000, when the scaling of planar MOSFET was approaching its end. Because of the physical locations of the inversion layers (at the sidewalls of the vertical fin), the convention of the device metrics of FinFET is slightly different from that of planar MOSFET. For example, the channel width of FinFET is usually referred to the fin height. Given that, both sides of the fin are inverted when the device is at the on state, the effective width for carriers traveling from the source to the drain is twice the physical channel width of FinFET. In contrast, this effective width is the same as the physical channel width of planar MOSFET because only one side of

the channel near the gate can be inverted. This difference might lead to confusion when evaluating the device performance of planar MOSFET and FinFET.

Note the silicon channel of the DELTA transistor is separated from the silicon substrate by a layer of silicon oxide while the channel of FinFET transistor is directly connected to the silicon substrate.

For a smooth transition from planar MOSFET to FinFET, the fabrication of FinFET is similar with that of planar MOSFET. For example, the vertical fins of FinFET are still patterned by using optical photolithography and dry etch. The various functional modules used in FinFET are similar to what is being using in planar MOSFET, and such modules include gate dielectric, high-k metal gate, source-drain extension ion implantation, epitaxial highly-doped source/drain, and self-aligned metal via. The direction of the logic semiconductor industry is to improve the circuit performance by adopting the low-leakage FinFET device while minimizing the risk in design, yield, and reliability [19].

This also justifies why most of the mature and proven technologies in the process flow of conventional chip making are still used in FinFET fabrication. The most challenging part of manufacturing FinFET is the fin formation, which involves accurate patterning and low-damage dry etch. A FinFET with low roughness and high uniformity is desirable for lowing the interface traps and variability of metal-gate work function. The mobility of the channel is degraded by the traps at the interface between the gate dielectric and the channel. The variability of metal-gate work function impacts the threshold voltage of the device [20]. Additionally, because both sides of the fin channel are controlled by the gate, the channel control of FinFET is much better than that of planar MOSFET. The use of lightly-doped or even un-doped silicon channel is now possible, and thus enables higher drive current because of less carrier scattering by the dopants. Intel is the first semiconductor company that commercially sold silicon chips based on FinFET technology in 2012, although Intel called their FinFET a "Tri-gate Transistor". The first generation of 22-nm node FinFET made by Intel is shown in **FIGURE 3** [21, 22].

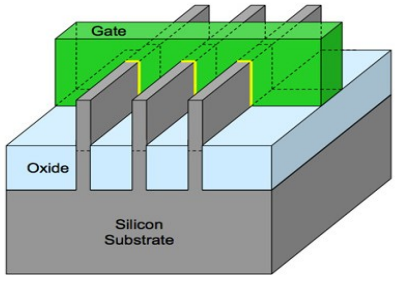


FIGURE 3. 22nm Tri-GATe Transistor [21]

The first generation of Intel's FinFET technology is the 22-nm FinFET shown in **FIGURE 4**(a). The fin width is 8 nm with rounded corners at the top of the fin. The rounded corner might be for reduction of the electric field near the corner for higher reliability, or simply a by-product of the fin etch process. The next generation of Intel's FinFET technology is the 14-nm FinFET shown in **FIGURE 4**(b). The fins became taller and thinner than the fins at 22-nm node. The corner is still somewhat rounded. The aspect ratio of the fin is higher which enables higher drive current and better off-state leakage control The latest 10-nm FinFET technology demonstrated by Intel in 2017 shows an even higher aspect ratio of the fin in **FIGURE 4**(c) [18, 21, and 23].

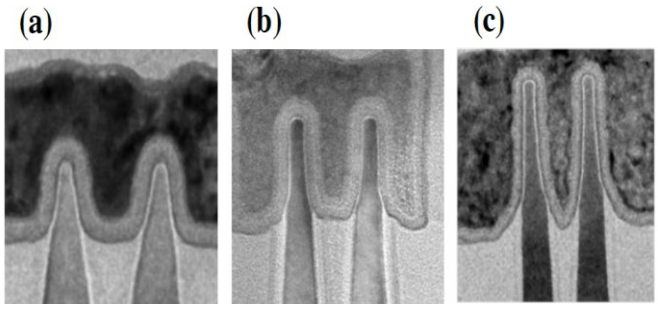


FIGURE 4. (a) Intel 1st generation FinFET at 22-nm node(2011) .(b) 2nd generation FinFET at 14-nm node (2013) . (c) 3rd generation FinFET at 10-nm node (2017) [23] .

Electrostatic Analysis of Gate All around (GAA) Nanowire over FinFET have been studied intensively by researchers in [23-24]. CMOS Technology has been scaled down to 7 nm with FinFET replacing planar MOSFET devices. Due to short channel effects, the FinFET structure was developed to provide better electrostatic control on subthreshold leakage and saturation current over planar MOSFETs while having the desired current drive. The FinFET structure has an unhoped or fully depleted fin, which supports immunity from random dopant fluctuations (RDF – a phenomenon which causes a reduction in the threshold voltage and is prominent at sub 50 nm tech nodes due to lesser dopant atoms) and thus causes threshold voltage (Vth) roll-off by reducing the Vth. However, as the advanced CMOS technologies are shrinking down to a 5 nm technology node, subthreshold leakage and drain-induced barrier- lowering (DIBL) are driving the introduction of new metal-oxide-semiconductor field effect transistor (MOSFET) structures to improve performance.

GAA field effect transistors are shown to be the potential candidates for these advanced nodes. In nanowire devices, due to the presence of the gate on all sides of the channel, DIBL should be lower compared to the FinFETs.

A 3-D technology computer aided design device simulation is done to compare the performance of FinFET

and GAA nanowire structures with vertically stacked horizontal nanowires [25]. Subthreshold slope, DIBL & saturation current is measured and compared between these devices. The FinFET's device performance has been matched with the compact model with the impact of tensile and compressive strain on NMOS & PMOS respectively. Metal work function is adjusted for the desired current drive. The nanowires have shown better electrostatic performance over FinFETs with excellent improvement in DIBL and subthreshold slope. This proves that horizontal nanowires can be the potential candidate for 5 nm technology node. A GAA nanowire structure for 5 nm tech node is characterized with a gate length of 15 nm. The structure is scaled down from 7 nm node to 5 nm by using a scaling factor of 0.7. MOS devices are compared based on various parameters for performance and reliability. At advanced technology nodes, power and delays can be considered as the dominant factors. For optimum performance of the devices, it is best to have minimum leakage and thus minimum subthreshold slope. The ideal SS, which can be obtained by a silicon device is 60 mV/dec. All the FinFET and similar devices have reached to ~65 mV/dec and still have some space for improvement. Due to DIBL, the threshold voltage of the device changes with a change in the power supply and thus metal gate loses full control on the channel. However, in analog circuits, to achieve the maximum gain, the slope of Id-Vd curve should be zero resulting in infinite output resistance of the transistor.

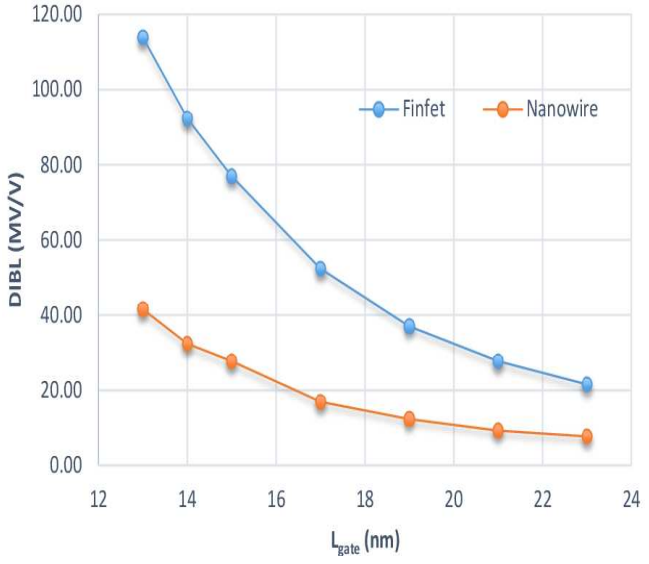


FIGURE 5. DIBL for NMOS FinFET & Nanowire [25]

Because of DIBL, all the transistors have a positive slope restricting the gain of analogue amplifier circuits. Moving towards 5 nm technology node, these parameters are getting worse resulting in the bad device performance. GAA nanowires are not immune to these short channel effects. But the question is whether semiconductor industry can move forward with GAA nanowires on the predicted scaling trend and can keep the Moore's law alive. A fair comparison is made between GAA nanowire and FinFET for DIBL. **FIGURE 5** shows the DIBL values for various gate lengths for both FinFET and nanowires. For gate length (L) = 21 nm, nanowire FET has DIBL ~10 mV/V, which is almost 0.4 times the FinFET having DIBL = 27.69 mV/V [25].

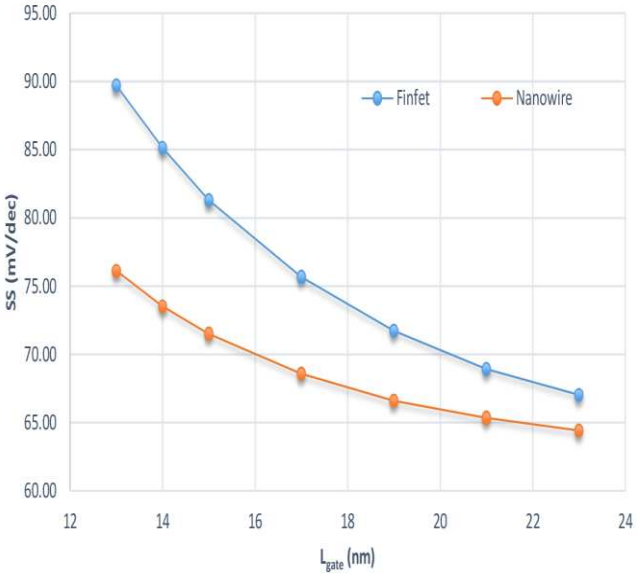


FIGURE 6. SS Calculated for NMOS FinFET & Nanowire [25].

According to the relation between gate length and DIBL of both FinFET and Nanowire Transistor, it is clear that the DIBL of nanowire with Gate length 15 nm shows the same amount of DIBL of FinFET with a gate length of 21 nm. Which leads to a ~28% of Lgate scaling, keeping the same device performance and maintaining the current drive.

For 5 nm technology, if we plan to have Lgate as 15 nm, DIBL for FinFET device becomes worse with a value 77 mV/V, which is more than twice the DIBL value at 21 nm Lgate. On the other hand, nanowire shows the same DIBL at Lgate = 15 nm, which FinFET has at Lgate = 21 nm The subthreshold slope for all the NMOS devices is shown in **FIGURE 6**.

It shows an increasing trend with decreasing channel length. For FinFET structure, the SS increases from 67.03 mv/dec to 89.7 mV/dec by sweeping the Lgate from 23 nm to 13 nm. Whereas for nanowire, the SS varies from 64.42 mV/dec to 76.13 mV/dec and do not show much variation. For scaling down to 5 nm, and at Lgate = 15 nm, nanowire shows the SS = ~71mV/dec. The SS of nanowire (Lgate = 15 nm) is not same as FinFET at Lgate = 21 nm.

Mobarakeh et al. [26] proposes a simulation study on three different nanowire FinFETs: Silicon, Germanium and SiGe nanowire FinFETs. This study try to find the logic performance parameters of these three structures such as

I_{on}/I_{off} ratio and DIBL the results indicates that the silicon structure show a significant characteristics compared to two other structures. This research study the influence of the parameters like dielectric thickness and the channel length in order to analyze and determine the short channel effects such as DIBL and also I_{on}/I_{off} ratio for switching application. It is shown that the performance can be improved by increasing ON current and then the I_{on}/I_{off} ratio in the structures can be improved by increasing the doping concentration and it also affects on DIBL. According to **FIGURES 7, 8, 9, and 10**, This study includes that the DIBL and I_{on}/I_{off} have a better performance with Si fin channel then SiGe, and the FinFET with Ge has a higher DIBL and lower I_{on}/I_{off}. Also it can concluded that the obtained results show that the SiGe FinFET is suitable for the analog application.

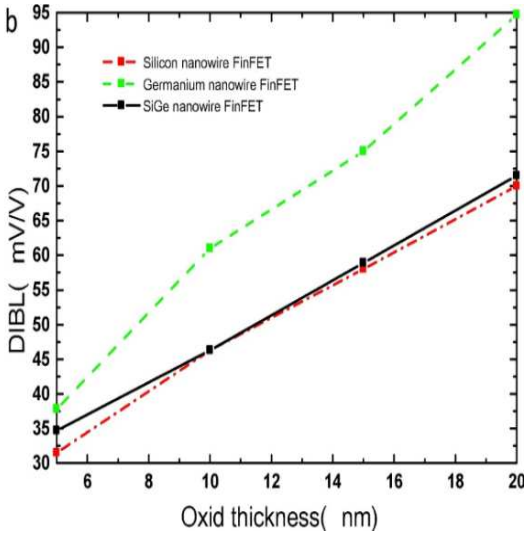


FIGURE 7. **Oxide thickness with DIBL [26].**

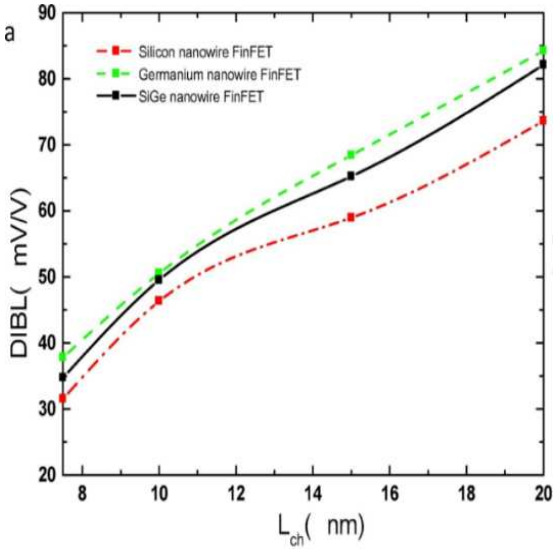


FIGURE 8. **Length channel with DIBL [26].**

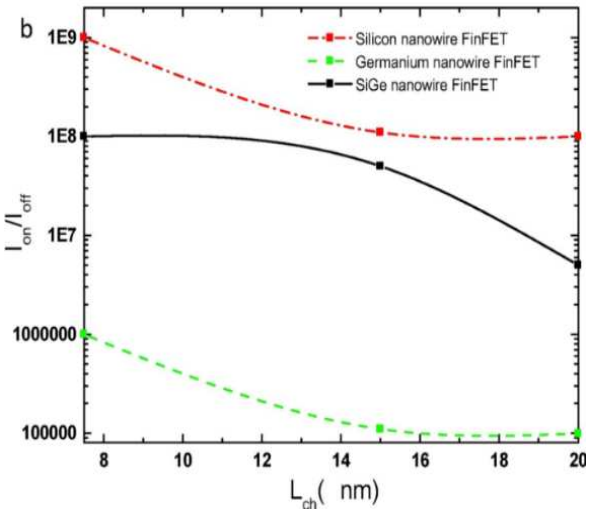


FIGURE 9. **Length channel with I_{ON}/I_{OFF} [26]**

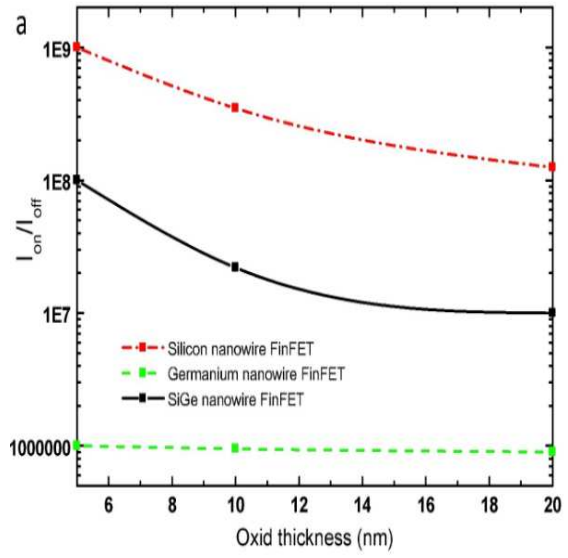


FIGURE 10. **Oxide thickness with I_{ON}/I_{OFF} [26]**

Effects of working temperature on MOS structure and its electrical parameters has been studied and well expressed in many research papers [27-30], FinFET temperature characteristics has been investigated by [28, 30], based on transfer characteristics of FinFET at drain voltage (Vd=1V) were investigated with different working temperature (-25, 0, 25, 50, 75, 100, and 125°C) with Si, Ge, GaAs and InAs as a semiconductor channel. The final results indicate that the I_{on}/I_{off} decreased (**FIGURE 11**) with increasing working temperature for all semiconductors channel types, but with best temperature stability with InAs and best temperature sensitivity with Si.

The Si channel FinFET has the better electrical characteristics with working temperature as shown in **FIGURE 12** [30]. According to the results, the temperature

sensitivity of FinFET increases linearly with oxide thickness within the range of 1–5 nm, furthermore, the threshold voltage and drain-induced barrier lowering increase with increasing oxide thickness. Also, the subthreshold swing (SS) is close to the ideal value at the minimum oxide thickness (1 nm).

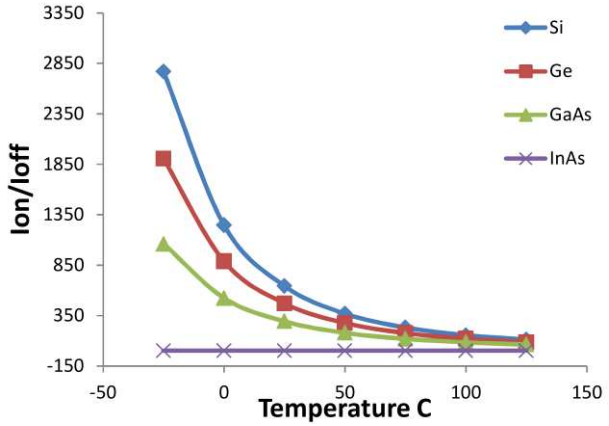


FIGURE 11. The I_{ON} / I_{OFF} temperature characteristics of FinFET with Si, Ge, GaAs and InAs as a semiconductor [29]

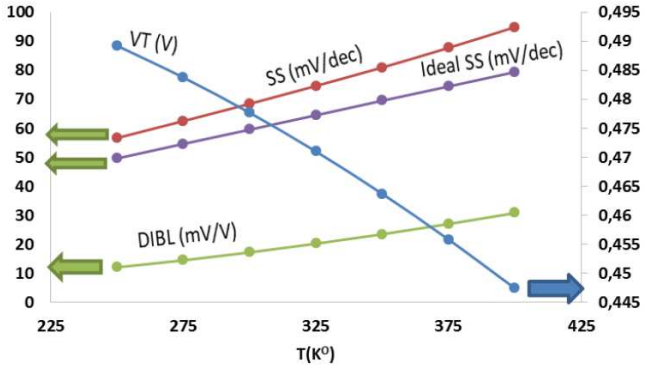


FIGURE 12. Electrical parameters of FinFET with working temperature [30]

III. CONCLUSION

The purpose of this study is to present and review the characteristics of FinFET structure to present how this structure overcome the problems of short channel effects in the traditional MOSFET structure. The finding of this research indicates that critical parameters of the characteristics of FinFET like ON to OFF current ratio, subthreshold swing and DIBL have excellent values. According to the nowadays nanotechnology, the manufacturing of the ICs will depend strongly on the FinFET structure.

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YASIR HASHIM (SMIEEE) received the B.Sc. and Master of Engineering in Electronics and Communications Engineering from the University of Mosul, Mosul, Iraq, in 1991 and 1995 respectively. He completed the Ph.D. in Electronics Engineering-Micro and Nano electronics from Universiti Science Malaysia (USM), Penang, Malaysia, in 2013. He is currently a Senior Lecturer in the Department of Computer Engineering, Faculty of Engineering, Tishk University, Erbil-Kurdistan, Iraq.