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DEVELOPMENT OF BUCK-BOOST CONVERTER TO ACHIEVE HIGH PF USING SERIES RESONANT CIRCUIT - PART I

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ABSTRACT:

The objective of this project work is to develop a Buck-Boost Converter to achieve high power factor with high operating frequency with simulation study. The recent technologies which involve high frequency applications such as wireless power transfer (WPT) use a high operating frequency in the range from a few hundred of kHz to over some of MHz. Such buck, boost or buck-boost configuration adopt improved power quality in terms of reduced total harmonic distortion (THD) of input current, power-factor correction (PFC) at AC mains and precisely regulated and isolated DC output voltage feeding to loads from few Watts to several kW. Further this paper presents a comprehensive study on power factor corrected single-phase AC-DC converter configuration, control strategy and design considerations, power quality considerations, latest trends, potential applications and future developments. Simulation results as well as comparative performance are presented and discussed for such proposed topology.

INTRODUCTION:

During recent years, resonant converters have gained renewed interest due to their advantages of higher efficiency, smaller size and weight for passive components and lesser EMI problems over the conventional PWM switching converters. Though they had been present for a long time, their applications were limited until the advent of high speed, low cost, controllable power semiconductor switches. Now a days, resonant converters are widely used for switching power supplies, AC motor drives and various other applications. It is widely perceived as the best candidate for the next generation of power converters.

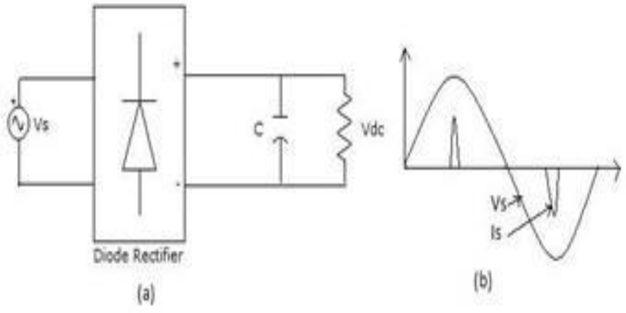

Fig. 1 Diode rectifier circuit with result

For rectification purpose the simplest approach is to use a diode rectifier circuit with an output storage capacitor, as shown in Fig. 1(a) [1]. In this circuit the capacitor is charged to a value close to the peak of the ac input voltage [see Fig. 1(b)]. Finally, pulsating input current of large magnitude occurs near the peak of the ac input voltage. Because of distorted input current the wireless power does not flow continuously from the primary side of the WPT system to the output of the system. Thus such diode rectifiers result in a poor input power factor (PF).

Figure 2 shows simulation of such diode rectifier circuit. Input voltage is taken as 50 Vrms. The result is depicted in fig.3 which shows the distorted input current with that of sinusoidal input voltage.

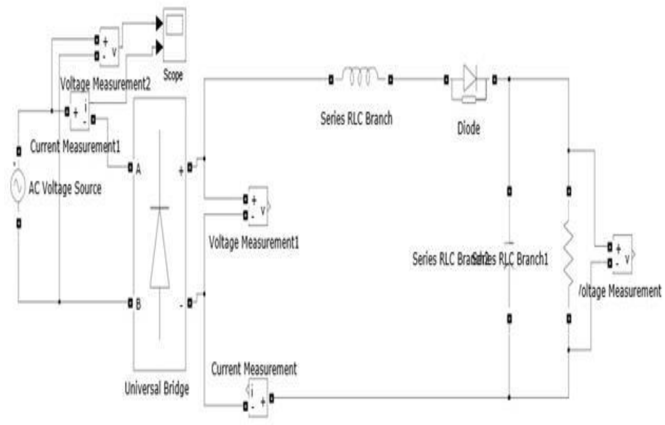

Fig. 2 Simulation Model Of Diode Rctifier

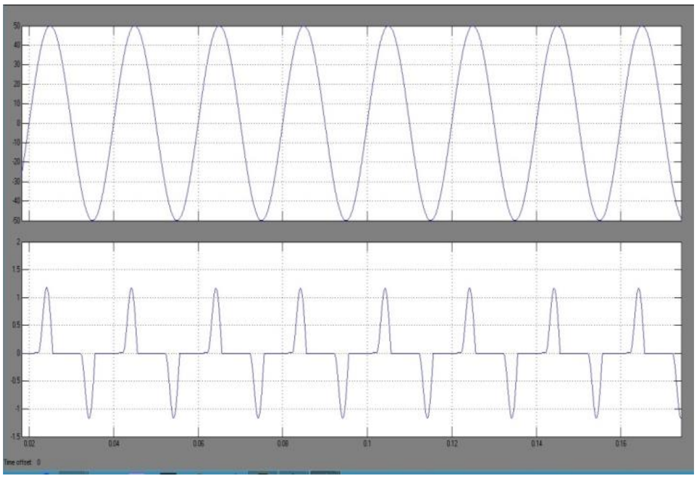

Fig. 3 Input voltage and current waveform

In order to overcome such problem of rustication, an excessive use of AC-DC converters in a number of applications have been increased. As a result, the power quality has become important to maintain clean power supply to the consumers. Depending upon the voltage levels, the AC mains voltage is converted into DC power to feed variety of loads through these single-phase isolated AC-DC converters, classified into three major categories, namely, single-phase buck, boost, and buck-boost configurations with improved power quality at input AC mains and output DC load.

LITERATURE REVIEW:

In modern industrial technologies including electronics and telecommunication, aerospace etc., a wireless power transfer (WPT) has been widely adopted with a high operating frequency in the range from a few hundred of kHz to over 10 MHz [1]. Recently, much research effort has been devoted to improving the performance of WPT systems in terms of transfer distance and systems energy efficiency. There is a lack of research targeting the optimal design of the power converter at the receiver side. This paper presents a power converter and its control circuit for high-frequency-fed ac to dc conversion. Based on the resonant technique, the input current is shaped to be sinusoidal and is forced to follow the high-frequency sinusoidal input voltage so as to achieve unity power factor. With the proper selection of the characteristic impedance of the resonant tank, the converter is able to perform the function of a buck, boost, or buck-boost converter. The initial condition of the resonant tank is used to control the output voltage gain of the converter. Since all the switches are operated at the fundamental frequency of the input ac source, the switching loss of the converter is small. A control scheme is also proposed for the converter. A proof-of-concept prototype operating at 400 kHz is constructed and its performance is experimentally measured.

In [2], the use and design of a Boost pre-regulator for the Power Factor Correction and the design, use and analysis of Buck Converter for power Factor Correction are described. Also comparision of various DC-DC Converter topologies for Power Factor Correction is described. The basic purpose of a Power Factor Correction circuit is to make the line current follow the waveform of the line voltage so that the input to the power supply becomes purely resistive or behaves like a resistor and hence to improve the power factor. This project work makes the use of Buck Converter in the Power Factor Correction circuit so as to improve the power factor of proposed system.

In [3], presents a comprehensive study on state of art of power factor corrected single phase AC-DC converters configurations, control strategies, selection of components and design considerations, performance evaluation, power quality considerations, selection criteria and potential applications, latest trends, and future developments. Simulation results as well as comparative performance are presented and discussed for most of the proposed topologies.

Interleaved buck and boost converters have been studied in recent years with the goal of improving power-converter performance in terms of size, efficiency, conducted electromagnetic emission and also transient response. The gains of interleaving consist of high power potential, modularity and better reliability. Since the inductor is frequently the largest and heaviest component in a high-boost converter, the use of a coupled inductor as a substitute of multiple discrete inductors is potentially beneficial [4]. The coupled inductors also offer additional benefits such as reduced core and winding losses as well as better input and inductor current ripples. Generalized steady-state analysis of multiphase IBCs has been previously reported.

PROPOSED PFC TECHNIQUE WITH BUCK-BOOST CONVERTER:

In proposed system an improved boost converter circuit is connected after a diode bridge rectifier to form a PF correction (PFC) circuit as shown in fig.4. The output dc voltage is sensed and fed to an error amplifier [1]. The difference between the actual and reference voltage is derived and applied to a compensator circuit such as a proportional-integral (PI) compensator. The output of the compensator is multiplied with the signal proportional to the ac voltage waveform Vs to produce the reference current signal I_{Lref}. After- ward, a current mode controller is used to generate the ON and OFF signal to the switch shaping the current waveform of the inductor. Therefore, the average wave shape of the ac current is forced to follow the waveform of the ac voltage.

This proposed scheme is simulated as shown in fig.5 with input voltage of 50 V at frequency 50 Hz. Thus we get the perfect sinusoidal input current with respect to input voltage and we are getting the unity power factor as shown in fig.6.

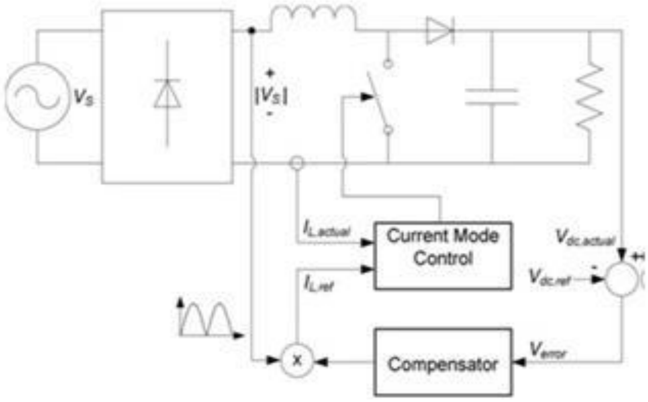

Fig. 4 PFC circuit

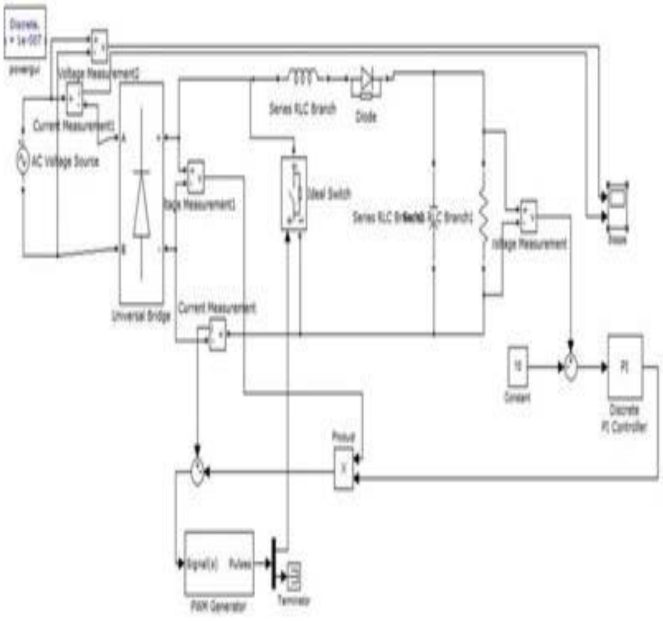

Fig. 5 Simulation of PFC circuit

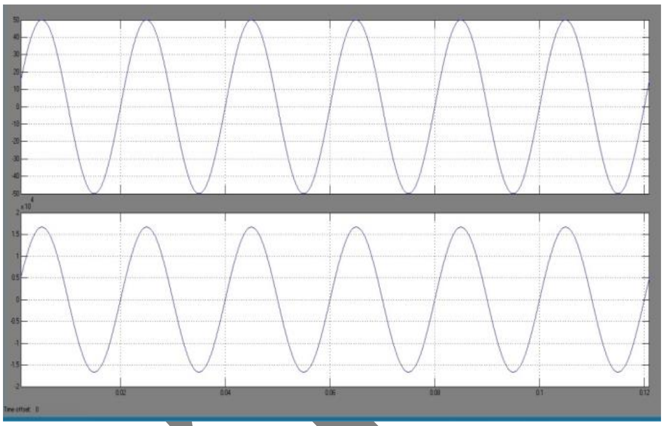

Fig.6 Result of PFC showing input voltage and input current

PROPOSED CONVERTER WITH PFC TECHNIQUE:

Following fig.7 shows proposed high frequency fed buck-boost converter circuit. The PF conditioning property is performed using the LC series resonant circuit at the input stage. The operation of the positive half cycle is used to describe how the LC resonant circuit can perform PF control in the high-frequency ac-dc power converter. A simplified circuit diagram is shown in Fig. 7.1.

Assume that the source frequency is the same as the resonant frequency of the LC circuit,

$$(\omega = \omega r = 1/[2\pi(Lr\ Cr\ )^{0.5}\ ] \quad \text{..........................} \quad (1)$$

and the initial current of the resonant inductor is zero. There are two parameters that will affect the amplitude and waveform of the inductor current. The first parameter is the equivalent impedance of the LC circuit which is designed by the resonant inductor and capacitor such that,

$$Z_{LC} = (Lr\ /Cr\ )^{0.5} \quad \text{..........................} \quad (2)$$

and the second parameter is the initial voltage of the resonant capacitor.

In [1] the current and voltage waveforms of the LC resonant circuit with different equivalent impedances in the positive half cycle of the input voltage. The initial voltage of the resonant capacitor and the current of the resonant inductor are zero.

$$(V_{Cr,init} = 0,\ I_{Lr,init} = 0) \quad \text{............................} \quad (3)$$

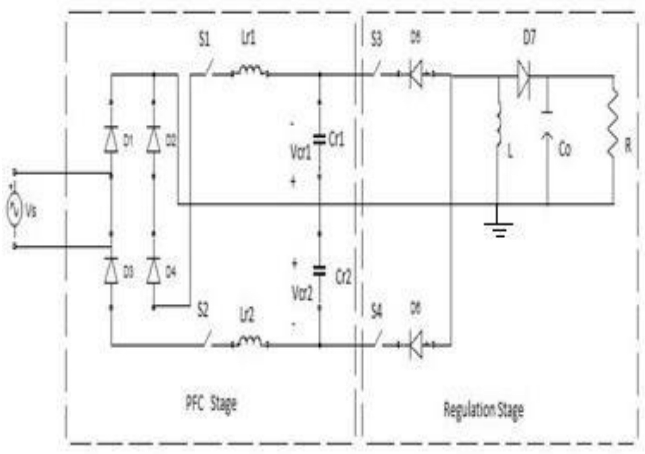

Fig.7 Proposed ac-dc Buck-Boost converter with PFC and Regulation stage

It can be observed that the source current is affected by the equivalent impedance of the LC circuit while the voltage waveform of the resonant capacitor remains the same. The total energy stored in the resonant capacitor over the positive half cycle is proportional to the size of the capacitance. Also the positive half cycle of the input voltage, the current of the resonant inductor, and the voltage of the resonant capacitor of the same circuit but with different initial conditions are depicted. It can be seen that the initial voltage value of the resonant capacitor can affect the magnitude of the resonant current of the inductor, of which the lower the initial resonant capacitor voltage, the higher the resonant inductor current becomes, and the lower the initial resonant capacitor voltage, the higher the capacitor voltage becomes at the end of the half cycle.

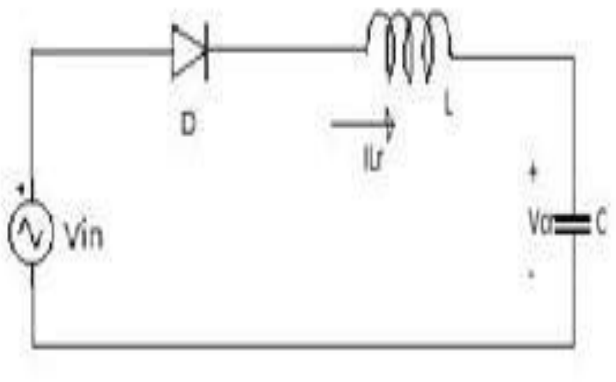

Fig. 7.1 Series resonant circuit

TIMING DIAGRAMS AND MODES OF OPERATION:

The timing diagrams of the proposed high-frequency-fed ac to dc power converter are shown in Fig.8. It can be seen that there are four operating modes as shown in Fig. 9 to 12. In the PFC stage, switches S1 and S2 are used to select the resonant tanks Lr1 Cr1 and Lr2 Cr2 for the positive and negative half cycles, respectively. In the regulation stage, S4 and S3 are the switches for controlling the buck boost converter for the positive and negative half-cycles, respectively. Here, it is assumed that Cr1 = Cr2 and Lr1 = Lr2 .

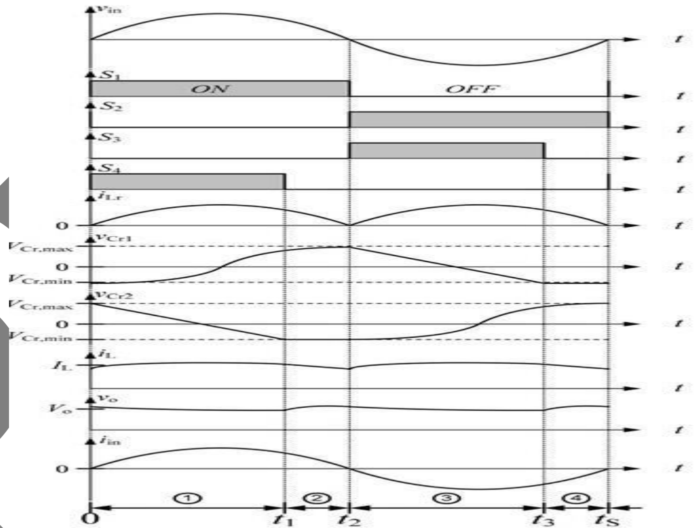

Fig. 8 Timing diagram

Mode 1 (t : 0 to t1): Initially the capacitor Cr1 and Cr2 are assumed to be charged to V_{Crmin} and V_{Crmax} , respectively. Then the positive half-cycle begins at t = 0. In the PFC stage, switch S1 is turned ON and switch S2 is turned OFF. Diodes D1 and D4 are in the conducting state but diodes D2 and D3 are not conducting [Fig.9]. Lr1 and Cr1 are connected in series to form a series resonant circuit. In the first positive half cycle the resonance takes place and the inductor current starts from zero and follows the first half of a sinusoidal waveform and then decreases to zero when D1 and D4 block the reverse current flow. In this span t= t1 the voltage of Cr1 is charged from its initial value V_{Crmin} to a certain level.

While regulating, switch S4 is turned ON and diode D6 is in its conducting state. Switch S3 is turned OFF and diodes D5 and D7 are reverse biased. The current iL can be assumed to be a constant magnitude because of large value of L. Capacitor Cr2 and inductor L form a closed circuit. Due to reverse polarity of D6 , Cr2 is discharged in one direction until the voltage of capacitor Cr2 is equal to the minimum voltage of capacitor Cr2 ($V_{Cr,min}$). The minimum voltage of capacitor Cr2 is either a positive voltage ($V_{Cr,min} > 0$), zero voltage ($V_{Cr,min} = 0$), or negative voltage ($V_{Cr,min} < 0$) depending on the output power. Energy is transferred from the PFC stage to the regulation stage and is stored in the inductor L. In this time period, the output capacitor CO delivers energy to the output load resistor RL.

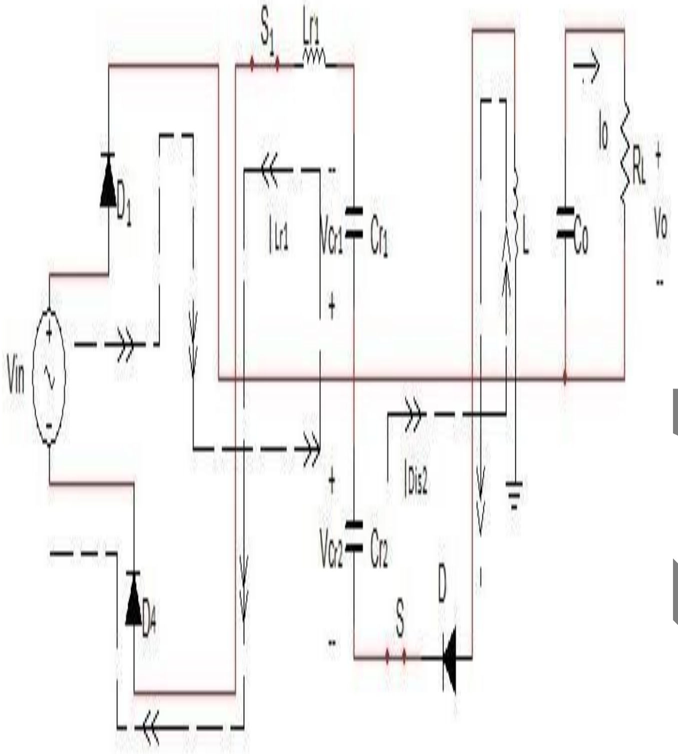

Fig.9 Mode 1

Mode 2 (t : t1 to t2): In the PFC stage, the functions of the switches (S1 and S2) and diodes (D1 , D2 , D3 , and D4) are the same as that in Mode 1. Thus, the capacitor Cr1 is kept charging by the power source to the level V_{Crmax} at t = t2 , at which the positive cycle ends. Now, ILr1 becomes zero and the switch S1 is commutated OFF naturally. The diodes D1 and D4 become non conducting. In the regulation stage, S3 and D5 remain in the OFF state. S4 is turned OFF at t = t1 and D6 is reverse biased when the voltage of Cr2 is equal to V_{Crmin} . Now, capacitor Cr2 is not connected to the PFC or the regulation stage. The current of inductor L cannot be changed instantaneously, resulting in the forward-biased conduction of diode D7 . Therefore, the energy stored in inductor L is delivered to the output capacitor C0 and the load resistor RL .

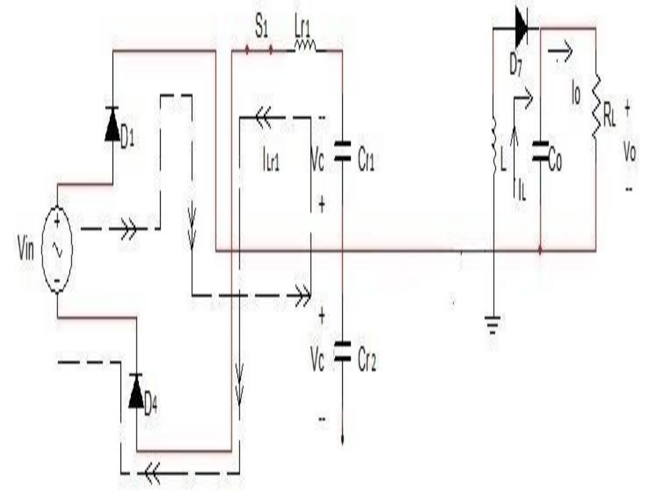

Fig. 10 : Mode 2

Mode 3 (t : t2 to t3): Next, in the PFC stage, switch S2 is turned ON and switch S1 is turned OFF. Diodes D2 and D3 are in the conducting state while diodes D2 and D3 are reverse biased [Fig.11]. Resonant tank Lr2 Cr2 is connected in series with the input source Vin . The input current Iin is shaped as a sinusoidal waveform. The voltage on capacitor Cr2 is charged from the initial value V_{Crmin} to V_{Crmax} . Energy is transferred from the input source Vin to capacitor Cr2 . In the regulation stage, switch S4 and diode D6 remain in the OFF state. Switch S3 is turned ON. Diode D5 is in the conducting state whileD7 is reverse biased. The energy stored in resonant capacitor Cr1 is transferred to inductor L. Cr1 is discharged to L until the voltage of capacitor Cr1 is equal to V_{Crmin} . Similarly to Mode 1, the load resistor RL is supplied by the output capacitor Co. In this way in the negative half-cycle of Vin, the negative part of the waveforms are similar to that of the positive half-cycle.

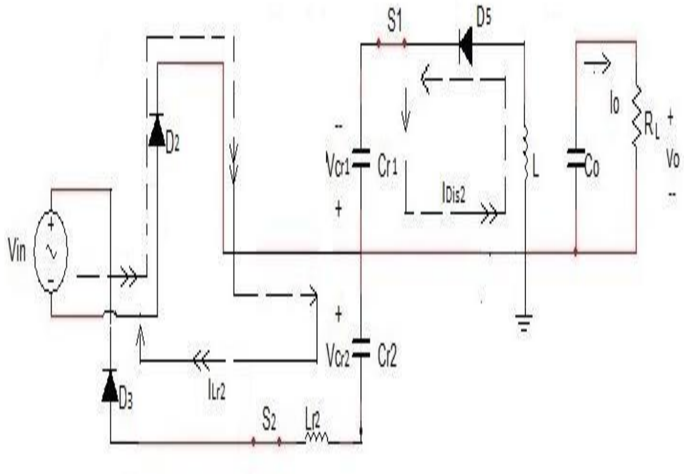

Fig. 11 : Mode 3

Mode 4 (t : t3 to ts): The switching state of the switches (S1 and S2) and diodes (D1 , D2 , D3 , and D4) are the same as that in Mode 3 in the PFC stage. At t = t3, in the regulation stage, switch S3 is turned OFF when the voltage of Cr1 is equal to V_{Crmin} . Energy stored in inductor L is transferred to output capacitor Co and load resistor RL through diode D7. Its equivalent circuit diagram is shown in Fig.12. Switch S2 is commutated OFF naturally when input source Vin becomes positive at t = t_S . Again the positive part of the operation is repeated and switches S1 and S4 are turned ON.

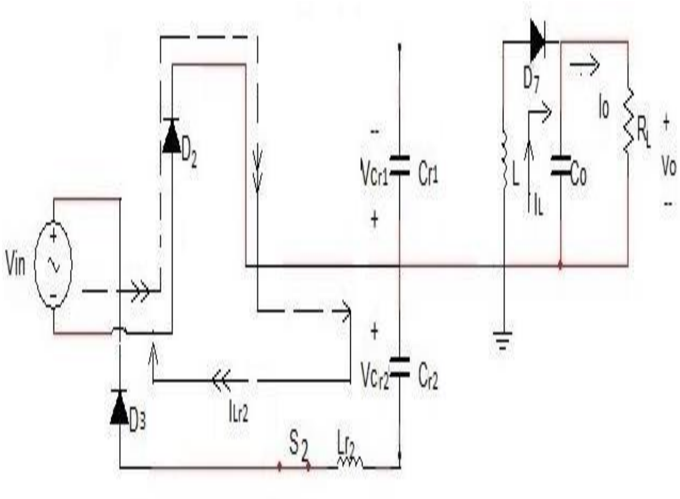

Fig. 12 : Mode 4

CONTROL METHODOLOGY:

Fig. 13 shows the control block diagram of the proposed high frequency- fed ac dc power converter. In the PFC stage, the ac source voltage Vin is sensed and fed to a phase detector circuit as shown in Fig.14. The outputs of the phase detector circuit are connected to the driver circuit to control the ON/OFF time of switches S1 and S2 following the ac source frequency. The signals Crt- S1 and Crt-S2 are the control signals of switches S1 and S2, respectively.

The outputs of the phase detector are also applied to the pulse-width modulation generator to derive the control signals Crt-S3 and Crt-S4 for switches S3 and S4 respectively. The instantaneous output voltage VO is sensed and subtracted from the reference output voltage V_{Ref} , of which the error is applied to a compensator to generate the threshold voltage VCr,min for the resonant capacitors Cr1 and Cr2 . Fig.14 also shows the control circuit of the regulation stage where the instantaneous voltage of the resonant capacitors VCr1 and VCr2 are being sensed and compared with VCr,min to generate the pulse width of the switches S3 and S4 .

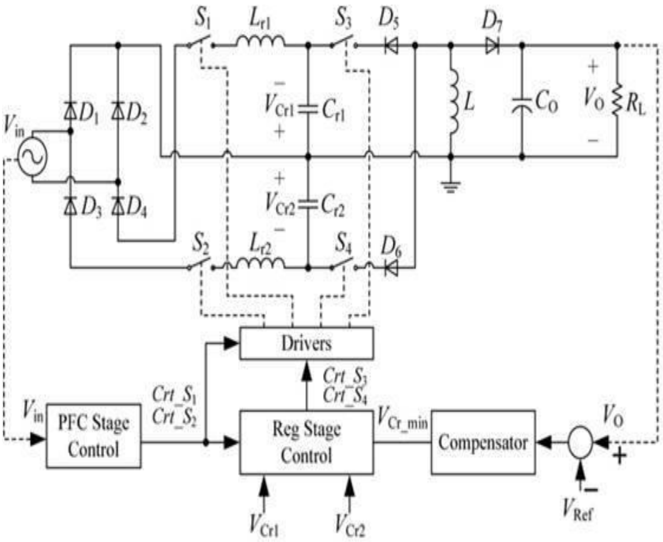

Fig. 13 Overall control block diagram

It is important to note that the proposed control circuit can be realized using simple operational amplifiers and digital logic gates. Consequently, they can be easily fabricated as an integrated circuit (IC) for mass production.

CALCULATION:

Calculation of the components used in simulation study are given in following table no.1. These components have been designed for buck operation of the proposed converter. The component calculation can vary as per the required operation, i.e. buck or boost in case of simulation.

Table no.1: Component Calculation

Sr. No.	Component	Symbol	Values
1	Resonant Inductor	L_r	2.02mH
2	Resonant Capacitor	C_r	20nF
3	Filter Inductor	L	0.6µH
4	Filter Capacitor	C	1.6mH

Fig. 16 shows the results of overall converter block diagram which is depicted in fi. 15. The first waveform shows input ac voltage, second the input ac current following the ac voltage waveform with some power factor correction. The third waveform is showing constant dc voltage with buck operation and the last; constant dc current with output power in few watts. We can increase this result with several kW further by selecting components with boost operation.

SIMULATION PART OF ENTIRE CONVERTER CIRCUIT:

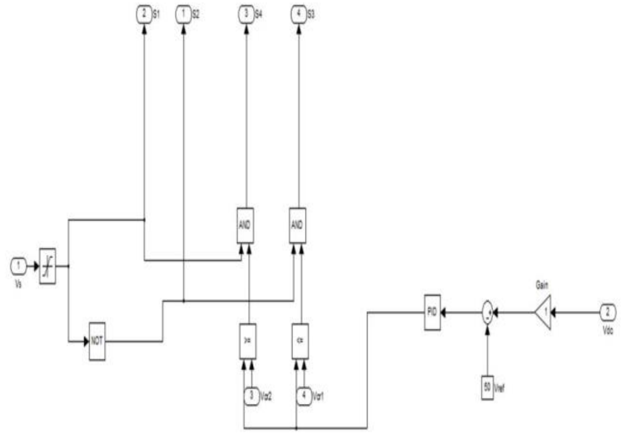

Fig.14 Simulation of control circuit

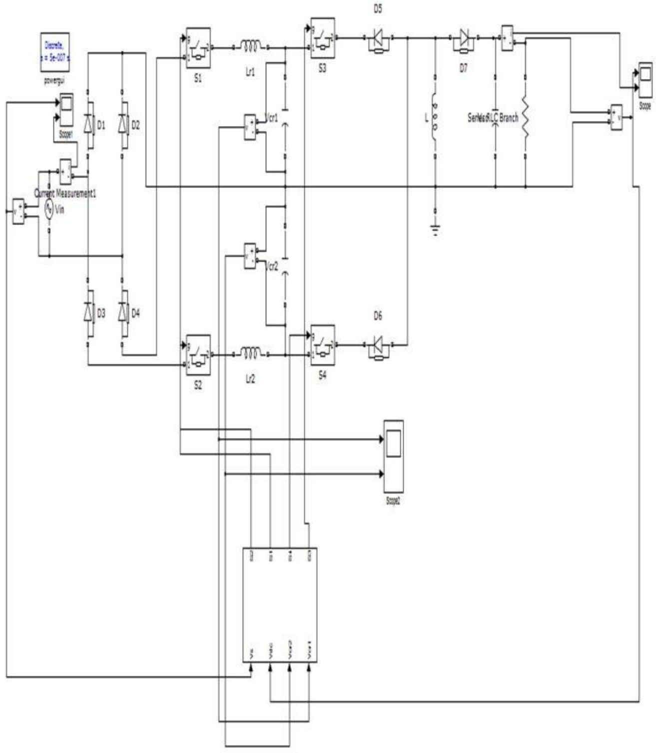

Fig. 15 Simulation of overall control block diagram

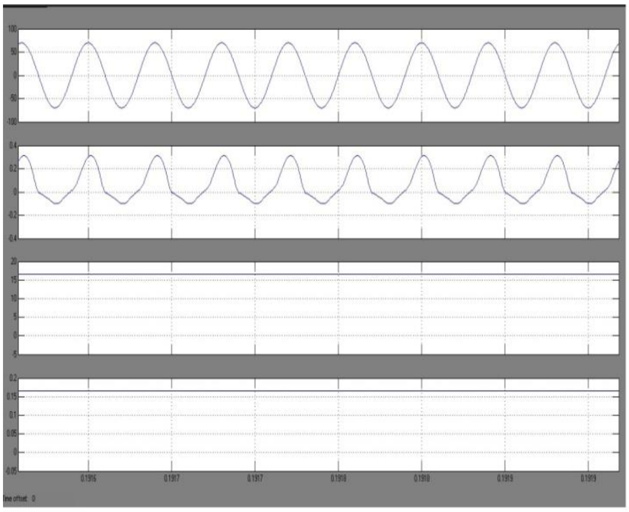

Fig.16 Simulation results with buck operation: Vin, Iin, Vdc, Idc resp.

CONCLUSION:

This paper presents a buck-boost power converter and its control circuit for high-frequency-fed ac to dc conversion based on simulation study. Based on the resonant technique, the input current is shaped to be sinusoidal and is forced to follow the high-frequency sinusoidal input voltage so as to achieve unity power factor. With the proper selection of the characteristic impedance of the resonant tank, the converter is able to perform the function of a buck, boost, or buck-boost converter. The initial condition of the resonant tank is used to control the output voltage gain of the converter. Since all the switches are operated at the fundamental frequency of the input ac source, the switching loss of the converter is small. A control scheme is also proposed for the converter. A proof-of-concept prototype operating at 25 kHz is being constructed and its performance will experimentally be measured which is left for further work.

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