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MODIFIED INPUT SCANNING METHOD USED TO 32 BIT X 32 BIT MULTIPRECISION MULTIPLIER

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Abstract-In this paper, we present a multiprecision (MP) reconfigurable multiplier that incorporates variable precision, parallel processing (PP), razor-based dynamic voltage scaling (DVS), and dedicated MP operands scheduling to provide optimum performance for a variety of operating conditions. Previous paper in used the PLL for the frequency division. If use the PLL for frequency division its hardware complexity increases .If frequency division is done by software using some frequency division method means hardware complexity is decrease and also speed is increases. All of the building blocks of the proposed reconfigurable multiplier can either work as independent smaller-precision multipliers or work in parallel to perform higher-precision multiplications. Given the user's requirements (e.g. throughput) a dynamic voltage/frequency scaling management unit configures the multiplier to operate at the proper precision and frequency.

Keywords- Computer arithmetic, dynamic voltage scaling, low power design, multi-precision multiplier.

I. INTRODUCTION

Nowadays, the demand for low power, high performance portable devices has been greatly increased. The growing market of portable electronic systems demands microelectronic circuits design with low power dissipation. The power dissipation mainly due to internal components [1]. In Digital Signal Processing applications, most frequently used arithmetic operation is multiplication. So Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, the following design targets – high speed, low power consumption and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power VLSI implementation.

Multipliers used in these applications have large area and consume considerable power. Therefore design of low-power multiplier has been an important part in low- power VLSI system design. A multiplier is an important part of digital signal processing systems, like frequency domain filtering (FIR and IIR), frequency-time transformations (FFT), Correlation, Digital Image processing etc. Multipliers have large area, long latency and consume considerable power. While many previous works focused on implementing high-speed multipliers, recently there have been many attempts to reduce power consumption. This is due to the increased demand for portable multimedia applications, which require low power consumption as well as high speed. There is wide range of multipliers. Based on the way the data is processed, they are classified as serial, parallel and serial-parallel multipliers.

Therefore, it is crucial to develop a multiplier with high performance but low power consumption. Multiplier is typically designed for a fixed maximum word-length to suit the worst case scenario. However, the real effective word-lengths of an application vary dramatically. The use of a non-proper word-length may cause performance degradation or inefficient usage of the hardware resources. In addition, the minimization of the multiplier power budget requires the estimation of the optimal operating point including clock frequencies, supply voltage, and threshold voltage [2].In most VLSI system designs, the supply voltage is also selected based on the worst case scenario. In order to achieve an optimal power/performance ratio, a variable precision data path solution is needed to cater for various types of applications. Dynamic Voltage Scaling (DVS) can be used to match the circuit's real working load and further reduce the power consumption.

II. HISTORY

An 8-bit multiplication computed on a 32-bit Booth multiplier would result in unnecessary switching activity and power loss. Many analyzed this word length optimization. They proposed an ensemble of multipliers of different precisions, with each optimized for a particular scenario. Each pair of incoming operands is routed to the smallest multiplier that can give the result to take advantage of the lower energy consumption of the smaller circuit. This ensemble the systems is reported to consume the low power but this came at the high cost, chip area given the used ensemble structure. To address this issue, [3] proposed to share and reuse some functional modules within the ensemble. In [3], an 8-bit multiplier is reused for the 16-bit multiplication, adding scalability without large area penalty. Extended this method by implementing pipelining to further improve the multiplier's performance. Combining multi-precision (MP) [1] with dynamic voltage scaling (DVS) can provide a reduction in power consumption. In proposed technique twin-precision is used rather than multi-precision array multiplier. Power and delay is reduced dramatically than multi-precision multiplier.

Due to the complex structure and interconnections, multipliers have large amount of unbalanced path which causes unwanted signal generation and propagation. This can be avoided by proper internal balancing through architectural and transistor level optimization.in most cases of multipliers, maximum word length is provided. Hence small multiplications are done in large multipliers, this causes unwanted switching activity and also power consumption. So word length optimization is the best method in which 8-bit multiplier is reused for 16-bit and 32- bit multiplication. Here it is possible to incorporate the pipelining for increasing the speed of the multiplier.

In conventional DVS technique, LUT tunes to supply voltages which are stored as predefined voltage and frequency relationship by considering all worst case conditions. It will consume more time and area. In razor based DVS technique, minimum voltage required for multiplication is found using razor based feedback and also many voltage transitions occurred during the calculation of particular product.

Due to this voltage transitions power consumptions and delay for product calculation is also increases. Because of dynamic voltage scaling unit, increased number of preemptions and frequency switching occurs which leads to worst case power consumption and delay and did not get optimum performance at various operating conditions. The previous work has many drawbacks. It takes more time for calculation of particular products and increased number of hardware components causes increased power consumption.

III PROPOSED TECHNOLOGY

Fig.1 shows over all multiplier system architecture. The overall multiplier system mainly consists mainly 5 units.

1) input operand scheduler which rearranges the input data and hence reduce the supply voltage transition, thus power consumption will be reduced.

2) MP multiplier is one which performs multiplication with variable precision and parallel processing.

3) Look Up Table is like a storage element used to store voltage required for multiplication.

4) Frequency scaling unit (FSU) which provides required frequency for the multiplication.

5) voltage and frequency management unit (VFMU) which is receives user requirement and control the LUT and FSU by giving suitable voltage and frequency for proper operation of MP
multiplier.

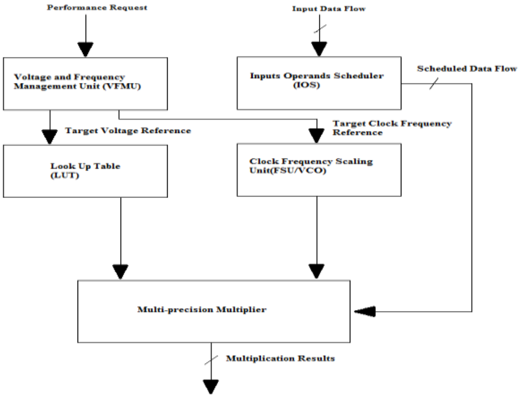

Performance Request
Input Data Flow
Voltage and Frequency Management Unit (VFMU)
Inputs Operands Scheduler (IOS)
Scheduled Data Flow
Target Voltage Reference
Target Clock Frequency Reference
Look Up Table (LUT)
Clock Frequency Scaling Unit(FSU/VCO)
Multi-precision Multiplier
Multiplication Results

Fig-1: Overall Multiplier System Architecture

All the five building blocks are working together to perform multiplication with variable precision. Input operands are given through IOS blocks which rearrange the inputs to reduce voltage transitions and given to the MP multiplier. This multiplier initially works at standard supply voltage of 3.3v. Since LUT stores the minimum voltage for each combinations, depending on the incoming operands precision adjust the input voltage suitable for that particular combination.

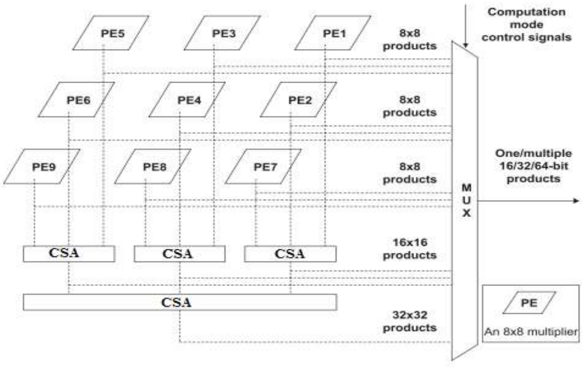


Fig-2: Possible configuration modes of MP multiplier

Fig 2 shows the proposed multiplier which consists nine 8x 8 bit multipliers. All these multipliers perform individual 8x8 bit operation and also can perform parallel multiplication for 16-bit and 32-bit multiplication. The processing elements of multiplier can either work as 9 independent multipliers or work in parallel to form 1, 2, or three 16 x 16 bit multiplier or a single 32- bit multiplication operation.

The pipelining method reduces delay and also gets fast multiplication result without error. Parallel processing is the ability of a device to simultaneously process incoming different inputs. Pipelining increases instruction throughput by performing multiple operations at the same time (concurrently), but does not reduce instruction latency (the time to complete a single instruction from start to finish) as it still must go through all the steps.

IV. MP RECONFIGURABILITY AND OVERHEAD

The structure of the input interface unit, which is a sub module of the MP multiplier as shown in Fig.2. The role of this input interface unit is to distribute the input data between the nine independent processing elements (PEs) of the 32 × 32 bit MP multiplier, considering the selected operation mode. The input interface unit uses an extra MSB sign bit to enable both signed and unsigned A 3-bit control bus indicates whether the inputs are 1/4/9 pair(s) of 8-bit operands, or 1/2/3 pair(s) of 16-bit operands, or 1 pair of 32-bit operands, respectively. Depending on the selected operating mode, the input data stream is distributed between the PEs to perform the computation. Fig. 2shows how three 8 × 8 bit PEs are used to realize a 16 × 16 bit multiplier. The 32 × 32 bit multiplier is constructed using a similar approach but requires 3 × 3 PEs. A 3-bit control word defines which PEs work concurrently and which PEs are disabled.

Whenever the full precision (32 × 32 bit) is not exercised, the supply voltage and the clock frequency may be scaled down according to the actual workload.

V METHODOLOGY

In block diagram consist of input operands schedeler,frequency voltage management unit, voltage scaling unit, frequency scaling unit, multiprecision multiplier.in this paper only focus on frequency division module .

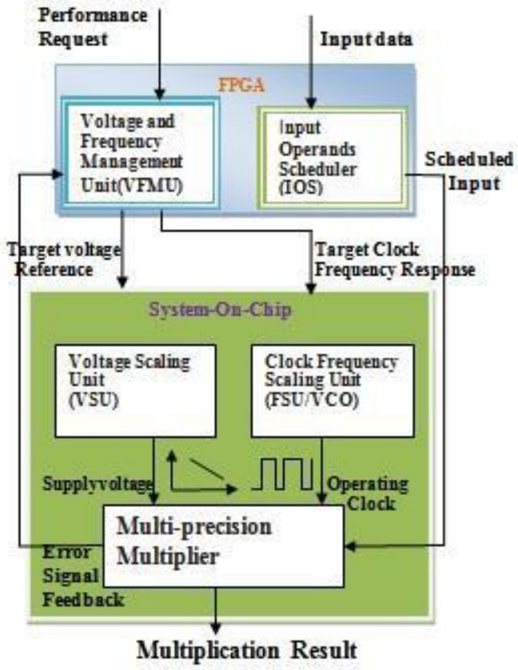

Performance Request
Input data
FPGA
Voltage and Frequency Management Unit(VFMU)
Input Operands Scheduler (IOS)
Scheduled Input
Target voltage Reference
Target Clock Frequency Response
System-On-Chip
Voltage Scaling Unit (VSU)
Clock Frequency Scaling Unit (FSU/VCO)
Supplyvoltage
Operating Clock
Multi-precision Multiplier
Error Signal Feedback
Multiplication Result

Fig 3.Overall multiplier system architecture

VI Frequency division

In this paper use the three multiprecision multiplier like 8x8bits,16x16bits and 32x32bits.The 8x8bits multiplier required less frequency as compare to the 16x16 bits multiplier and 16x16bits multiplier required less frequency as compare to 32x32bits multiplier. If 32x32bits multiplier require f frequency then 16x16bits require f/2 and 8x8bits require f/4 frequency.

In Previous paper used the PLL circuit for the frequency division it's very complex hardware, in this paper we replace the PLL by softwarly frequency division module. In this module we use the f frequency as the circuit frequency and is divide into the f/2,f4.

Below is the schematic diagram of the frequency division module. The main frequency is divide into the f/2,f/4 according to the control signal its generate from input operand scheduler.

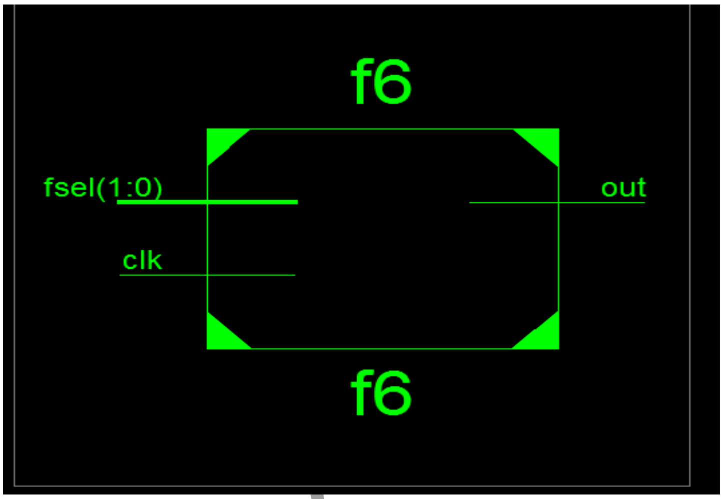


Fig 4. Schematic diagram of frequency division.

The clk is the main frequency and fsel is the control signal. Out is output signal.

If we select 01 mean frequency is f/4 its use for 8x8 bits multiplier.

If we select 10 mean frequency is f/2 its use for 16x16 bits multiplier.

If we select 11 mean frequency is f its use for 32x32 bits multiplier.

RESULT

1] First input:

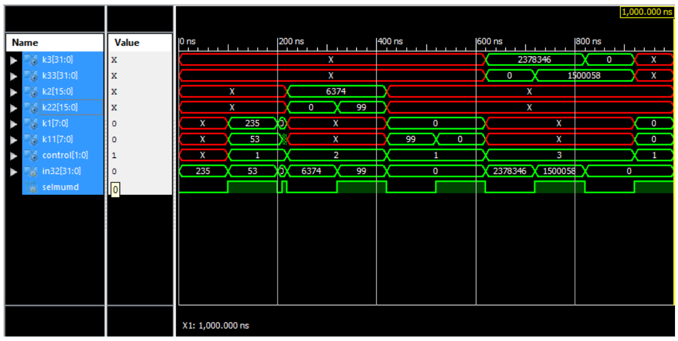
first select the selmud=0 and give input value to in32=56; after change the value of selmud=1 and again give the value to in32=135;the output is generate control signal=1 and k3=56 and k33=135 because both value of in32 is less than 256 that's via output is generate like that.

2] Second input:

first select the selmud=0 and give input value to in32=2456; after change the value of selmud=1 and again give the value to in32=756;the output is generate control signal=2 and k2=2456 and k22=756 because both value of in32 is less than 32768 that's via output is generate like that.

3] Third input:

First select the selmud=0 and give input value to in32=3562145; after change the value of selmud=1 and again give the value to in32=249632166;the output is generate control signal=3and k1=3562145 and k11=249632166because both value of in32 is greater than 32768 that's via output is generate like that.



Name	Value
k3[31:0]	X
k33[31:0]	X
k2[15:0]	X
k22[15:0]	X
k1[7:0]	0
k11[7:0]	0
control[1:0]	1
in32[31:0]	0
selmumd	0

CONCLUSION & FUTURE SCOPE

Here we present a Modified Input Scanning Method Used to 32 bit x 32 bit Multiprecision Multiplier. Further we are going to study a multiprecision (MP) reconfigurable multiplier that incorporates variable precision, parallel processing (PP), razor-based dynamic voltage scaling (DVS), and dedicated MP operands scheduling to provide optimum performance for a variety of operating conditions.

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