Reversible Full Adder Gate using Nano-technology

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Abstract— **Reversible logic has become one of the promising research directions in low power dissipating circuit design in the past few years and has found its applications in low power CMOS design, cryptography, digital signal processing, optical information processing and nanotechnology. This paper presents a quantum cost efficient reversible full adder gate in nanotechnology. This gate can work singly as a reversible full adder unit and requires only one clock cycle. The proposed gate is a universal gate in the sense that it can be used to synthesize any arbitrary Boolean functions.**

Index Terms— **CMOS, Peres Full Adder Gate (PFAG), BCD.**

I. INTRODUCTION

This paper presents a novel 4*4 reversible gate namely Peres Full Adder Gate (PFAG) , that is, it has 4-input lines and 4-output lines. This gate can be used to realize any arbitrary Boolean function and therefore universal. The hardware complexity of this gate is less compared to the existing ones and requires only one clock cycle. The quantum realization cost of this gate is only 8 and ready for use in current nanotechnology. Reversible logic design differs significantly from traditional combinational logic design approaches.

In reversible logic circuit the number of input lines must be equal the number of output lines, each output will be used only once and the resulting circuit must be acyclic . The output lines that are not used further are termed as garbage outputs. One of the most challenging tasks is to reduce these garbage's. Any reversible logic gate realizes only the functions that are reversible. But many of the Boolean functions are not reversible. Before realizing these functions, we need to transform those irreversible functions into reversible one. Any transformation algorithm that converts an irreversible function to a reversible one introduces input lines that are set to zero in the circuit's input side. These inputs are termed as constant inputs. Therefore, any efficient reversible logic design should minimize the garbage's as well as constant inputs.
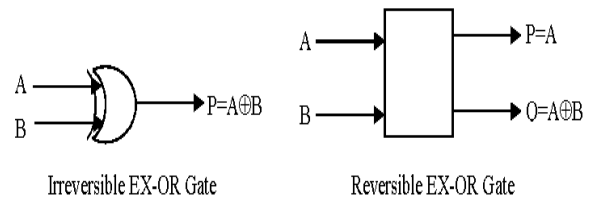
Figure 1: Irreversible and reversible gate

II. REVERSIBLE LOGIC GATES

There exist many reversible gates in the literature. Among them 2*2 Feynman gate , 3*3 Fredkin gate, 3*3 Toffoli gateand 3*3 Peres gate is the most referred. The detailed cost of a reversible gate depends on any particular realization of quantum logic. Generally, the cost is calculated as a total sum of 2*2 quantum primitives used. The cost of Toffoli gate is exactly the same as the cost of Fredkin gate and is 5. The only cheapest quantum realization of a complete (universal) 3*3 reversible gate is Peres gate and its cost is 4.
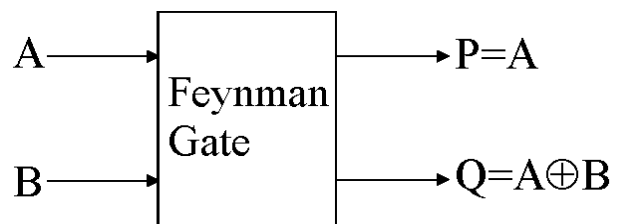

Figure 2: 2*2 Feynman gate

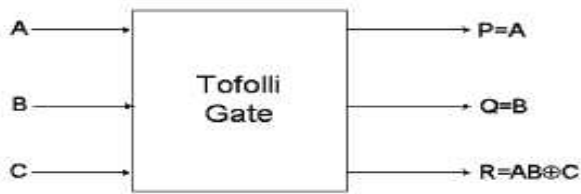
Figure 3: 3*3 Fredkin gate
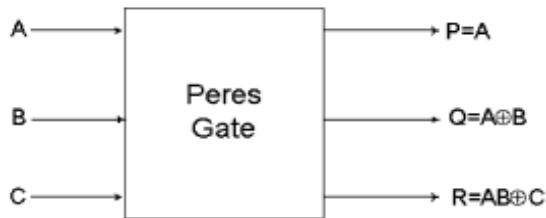
Figure 4: 3*3 Toffoli gate

Figure 5: 3*3 Peres gate

III. REVERSIBLE LOGIC IMPLEMENTATION OF FULL ADDER CIRCUIT

Full adder is the fundamental building block in many computational units. The anticipated paradigm shift logic compatible with optical and quantum requires compatible reversible adder implementations.

The full adder circuit's output is given by the following equations:

$$Sum = A \oplus B \oplus Cin$$
$$Cout = (A \oplus B)Cin \oplus AB$$

This implementation of reversible full adder circuit is also efficient in terms of gate count, garbage outputs and constant input than the existing counter parts.
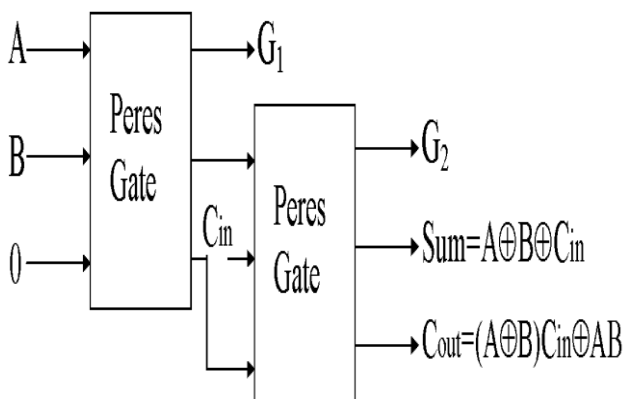

Figure 6: The only cheapest quantum realization of reversible full adder circuit

IV. REVERSIBLE FULL ADDER GATE

Full adder is the fundamental building block in almost every arithmetic logic circuit. Therefore, a gate that can work singly as a reversible full adder will be beneficial to the development of other complex logic circuits. This gate requires only one clock cycle and produces no extra

Garbage outputs, that is, it adheres to the theoretical minimum as established.
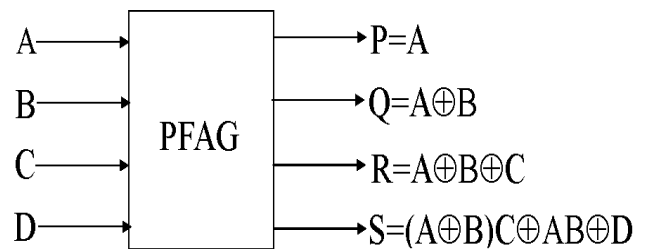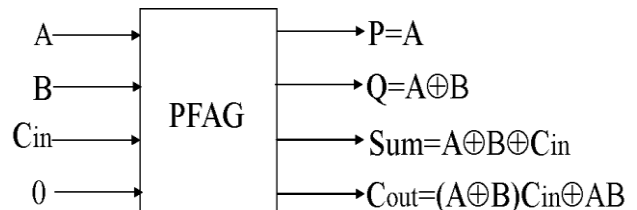

Figure 7: 4*4 Peres Full Adder Gate

Figure 8: PFAG gate as a reversible full adder circuit

The functionality of HNG and PFAG is almost similar except that PFAG provides half adder sum output besides of giving full adder sum output. This extra output will be advantageous to the development of other adder circuit such as carry skip adder and BCD adder. The quantum realization of TSG, HNG and MKG is not given in the literatures so far and is therefore unknown.

V. RESULTS

The following demonstrates that the proposed reversible full adder gate is superior to the existing counterparts in terms of hardware complexity, quantum costs, garbage outputs and constant inputs.

VI. CONCLUSION

This paper presents a new quantum cost efficient reversible full adder gate in nanotechnology. This gate requires only clock cycle and can be used to synthesize any arbitrary Boolean functions therefore universal. The hardware complexity offered by this gate is less than the existing reversible full adder gates. The quantum realization cost of this gate is only 8. This gate is readily available for use in nanotechnology since its quantum implementation is given in NMR technology.

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