Effective Test Pattern Generation using LFSR for Memory Testing

Dheeraj Singh, Deepak Agarwal, Gaurav Bargoti, Himanshu

Abstract— **With IC size shrinking smaller and smaller, it become more challenging to test semiconductor memories. Many defects cannot be accurately modeled using known fault models. The effectiveness of test methods for such circuits can therefore be measured in terms of the coverage obtained for unmodeled faults. A large proportion of the cost of memory comes due to testing of memory. And testing cost of the memory is the function of testing time which is directly proportional to each other . The purpose of this paper to proposed a technique to generate an effective test pattern by using Linear Feedback Shift Register which reduce the consuming time for testing the memory and also have higher defect or fault coverage. Here we describe the LFSR hardware by Verilog HDL to design its logic circuit and simulate its performance. LFSR have simple and compact structure and produce random pattern which essential for testing and hence its our first choice to implement the Test Pattern Generator (TPG) for BIST.**

Index Terms— **Verilog HDL, LFSR, TPG, Fault coverage , BIST .**

I. Introduction

Linear Feedback Shift Register is constructed using D-flipflop connected as a Shift Register with feedback path that are linearly related using X-OR gates which generate pseudo random sequence. There are two ways to implement LFSRs i.e. the linear element (X-OR gate) appears between flipflop or X-OR gates appear only in feedback path. Due to their simple and compact structure, they require very small area overhead and hence LFSR are widely adopted as Test Pattern Generator (TPG) and Output Response Analyzer (ORA) in the Built In Self Test (BIST) technique. For certain configuration of the LFSR , the sequence have an interesting property, to be more precise they are pseudo random. The sequence of vectors generated do not repeat except at interval of length 2^n-1 ,where n is the number of flipflops. In a truly random sequence , vector repeats at varying intervals and the same vector can appear twice in a row. Period should be very long for Memory Testing.

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Algorithmically generated test pattern provide good fault coverage , but have few disadvantage i.e. Test pattern generation is extremely time consuming , Storage is required to hold the test pattern , and the speed at which tests can be applied is limited. Testing speed is important not only because testing is a necessary step in manufacturing process , but because it is often deseriable to apply tests at operational speed. This limitation can be overcome by generating Test Pattern using LFSR.

II. Proposed Model

In this section we introduce new modified architecture of LFSR which extended the maximum length sequence beyond to 2^n-1 pattern with the manipulation of the D(x) clock. As we know that conventional LFSR TPGs will produce a maximum set of 2^n-1 number of test vector. In modified LFSR , the total number of test vectors is still a maximum of 2^n-1 , but there will be duplicate of certain vectors within the same sequence and increase the period of test pattern along with randomness in test pattern .

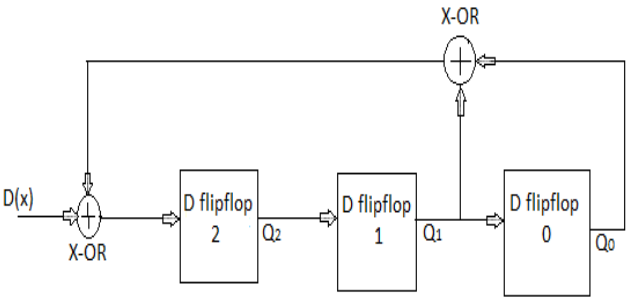

Figure 1 : Modified 3 stage LFSR Architecture

The test pattern are generated by a TPG using a standard LFSR with a characteristic polynomial of $x^3 + x^2 + 1$ and seed value of $Q_2\ Q_1\ Q_0 = 100$. The frequency of the D(x) clock is half of the register clock (T=2). From the table, we see that the maximum length sequence of the LFSR is 7 vectors. For the proposed LFSR TPG , the sequence extends to a total of 14 vectors before the sequence repeat itself which indicate that period of test pattern will increase and randomness in the test vectors are also enhance. Another important thing in this proposed model is that it is able to

generate the all zeros state autonomously and is not stuck in all zero state.

Table: 1

LFSR clock	Conventional LFSR Sequence	Modified LFSR sequence
0	100	100
1	010	010
2	101	001
3	110	100
4	111	110
5	011	111
6	001	111
7	100 (repeat)	011
8	010	101
9	101	110
10	110	011
11	111	001
12	011	000
13	001	000
14	100 (repeat)	100 (repeat)

Taking the frequency of the register clock as f ; and the frequency of the D(x) clock as $f_{D(x)}$. the ratio of the clocks is r =f / $f_{D(x)}$. For an r = 2 { D(x) frequency is half of register clock frequency } , the input at D(x) is effectively an alternating stream of 0`s and 1`s. This proposed TPG is capable of cycling through the all zeros state, it does not have own trivial sequence which will cause it to be stuck in a similar manner that a conventional LFSR is stuck at the all zero state.

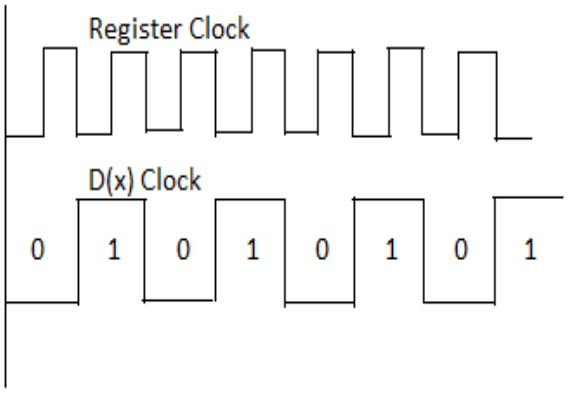

Figure 2 : Positive Edge Register clock with D(x) clock at half frequency

If the initial state of the LFSR is $Q_2 Q_1 Q_0$ = 100 and at the first register clock , the input at D(x) is 0, then the next LFSR state will be $Q_2 Q_1 Q_0$ = 010. If at the next register clock the input at D(x) is 1 , then the LFSR will switch to 001 and so on. Subsequently, an alternative stream of 0`s and 1`s will prevent the LFSR to be stuck at the zero states . This extra D(x) clock signal will avoid the stuck condion when zeros state arise (as arise in conventional LFSR).

III. Conclusions

In this study , we analyze 3 bit modified LFSR and we obtain the more random test pattern of large period than the conventional LFSR. The test pattern contain the same vector twice or thrice in a period and generate zeros state which does not stuck in all zero state. As we know that these property of modified LFSR Architecture can detect the unmodeled faults present in the memory. In the similar fashion we can generate more random test pattern by increasing the number of flipflop in LFSR structure to enhance the fault coverage.

References

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