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Design of Low Power Half Adder using Static 125nm CMOS Technology

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***Abstract*— The key components in digital design are Half adders.They perform not only addition operations, but also many other functions such as subtraction, multiplication and division. Very Large-Scale Integrated circuits (VLSI) frequently requires adders of various bit widths from processors to Application Specific Integrated Circuits (ASICs). Recently reported logic style comparisons based on full-adder circuits claims that the Complementary Pass transistor Logic (CPL) is much more power-efficient than complementarymetal oxide semiconductor(CMOS). However, new comparisons are performed on more efficient (CMOS) circuit realizations and a wider range of different logic cells as well as the use of realistic circuit arrangements demonstrates that the (CMOS) is superior to (CPL) in most cases with respect to speed, area, power dissipation, and power-delay products. Even Adder designed using (CMOS) complementary metal oxide semiconductor technology can have more power as well as speed than that using (CMOS) technology. The most important and widely accepted matrices for measuring the quality of adder designs power dissipation,propagation delay, and area. The overall performance can be significantly improved by using arithmetic circuits. This paper describes the comparative performance of half adder designed using TANNER (EDA) Electronic Design Automation, using different (CMOS) logic design styles.**

***Index Terms*— Half Adder, (CMOS), Tanner EDA,Logic DesignStatic**

I. INTRODUCTION

The basic building block in the arithmetic unit of digital signal processors and application specific integrated circuits used in various digital electronic devices is the adder.Half adder is a combinational arithmetic circuit which adds two inputs A & Band produces outputs as sum bit (S) and carry bit (C) as the output. If A and B are the input bits then sum bit (S) is the X-OR of A and B and the carry bit (C) will be the AND of A and B. From this it is clear thatusing one X-OR gate and one AND gate a half adder circuit can be easily constructed.Simplest of all adder circuit is the half adder, but it has a major disadvantages. The half adder can add only two input bits (A and B) and has nothing to do with the carry if there is any in the input. So if the input to a half adder have a carry, then it will be neglected and adds only the A and B bits. That means the binary addition process is not complete and that's why it is called a half adder.We have designed Half adder using (CMOS) technology.One of the most popular and broadly usedtechnology in the computer chip design industry is the Static (CMOS) technology to form integrated circuits in numerous and varied applications. Due to several key advantages today's computer memories, (CPUs) and cell phones make use of this technology. Both P channel and N channel semiconductor devices are used in this technology.We have designed four types of half adder namely [1] 3 AND INVERTOR OR GATE(3AIR), [2] 2AND2OR GATE (2(AR)), [3] NOT 2AND OR GATE

(N2AR) [4] NOT AND 2 OR GATE (NA2R),, Using a software called Tanner EDA. Tanner EDA tools comprises of many tools related to Electronic Circuits like S-Edit, W-Edit, Wave Tool, L-Edit etc. For Our Research We have used S-Edit, T-Spice and wave form software.

II. EXISTING SYSTEM:

Two binary inputs and two binary outputs are required by half adder circuits. The input variables designated the augends and added bits; the sum and carry are produced by the output variables.

The block diagram of half adder is shown in Fig-1

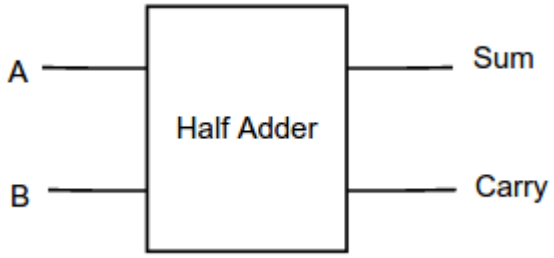

Fig-1: Block diagram of half adder

According to the truth table the simplified Boolean function is given as

S=A'B+AB'

C=AB

Table-1 gives the input output relation

Table-1 Truth table of half adder

Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

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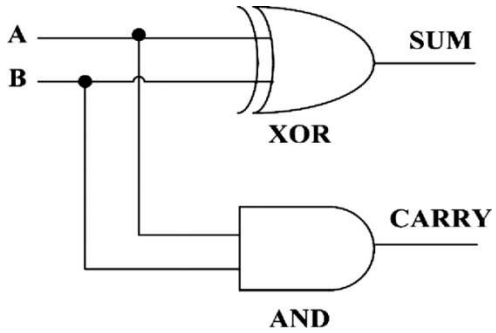


Figure 2. Simple half adder using XOR and AND gate

In Very Large Scale Integration circuits, an adder using XOR gates which are in turn designed with less number of transistors is implemented. The key idea for this design is modifying XOR gate portion in an adder using minimum number of transistors. The most fundamental blocks for building adder systems are the XOR gates. The performance of adder can be improved by designing XOR gate by using minimum number of transistors but without sacrificing the performance. Eight transistors or six transistors were used to design XOR gates in early designs.

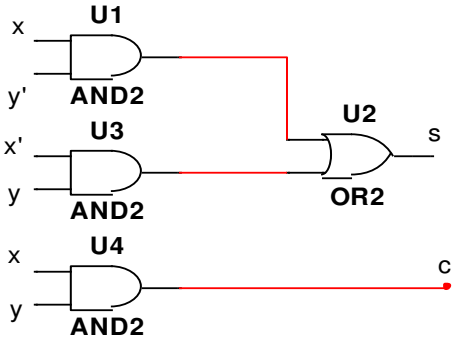
III. ADVANCED HIGH SPEED ADDER:

The advanced type of half adders are designed using the principle of the static (CMOS) technology. The main aim of this research is to make the size of fabrication more small in terms of nanometre. The (CMOS) comprises of (NMOS) and (PMOS).

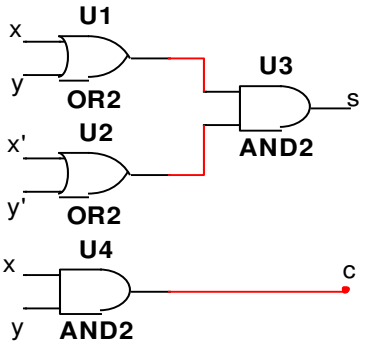
Types of Half Adders:

[1] 3AIR
[2] 2(AR)
[3] N2AR
[4] NA2R

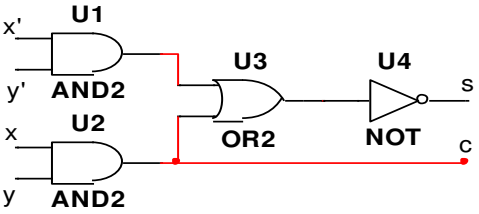
[1] 3AIR:



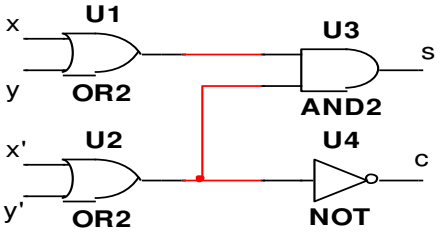
[2] 2(AR):



[3] N2AR:

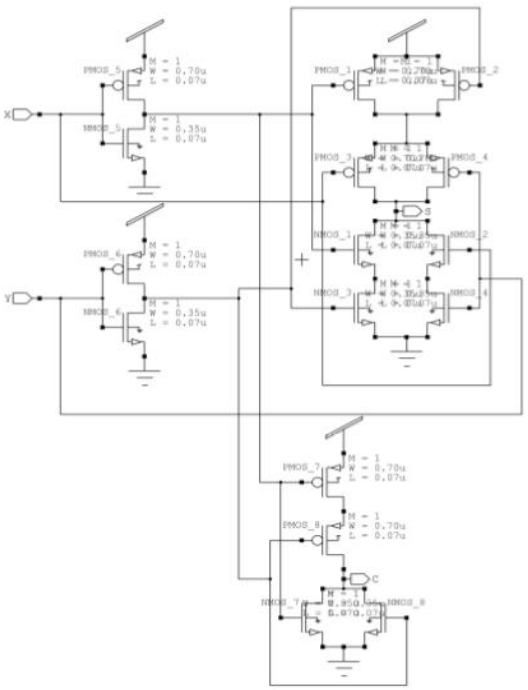


[4] NA2R:

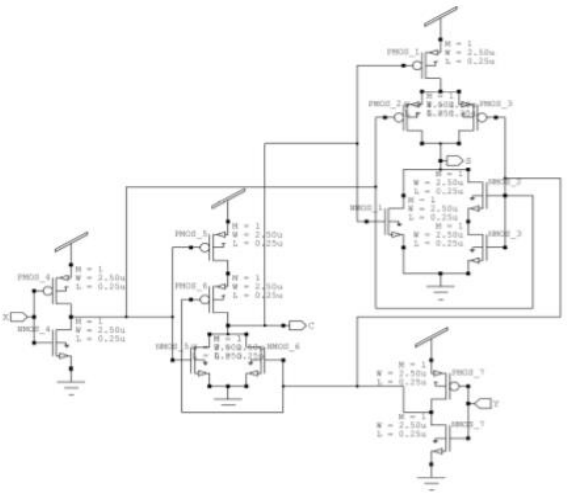


IV. RESULTS :

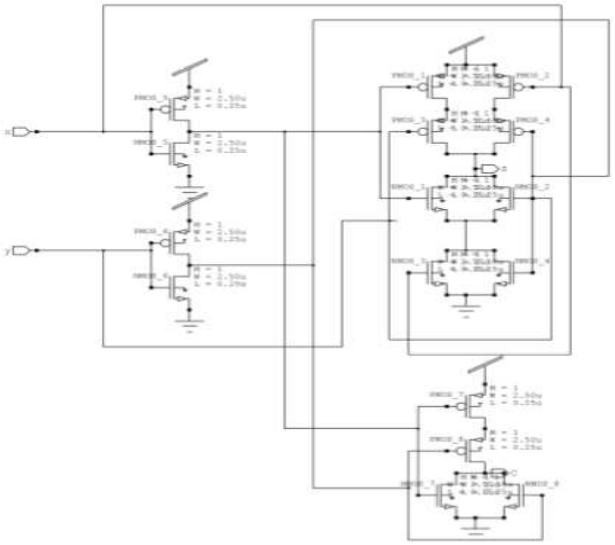
A.1 3AIR:



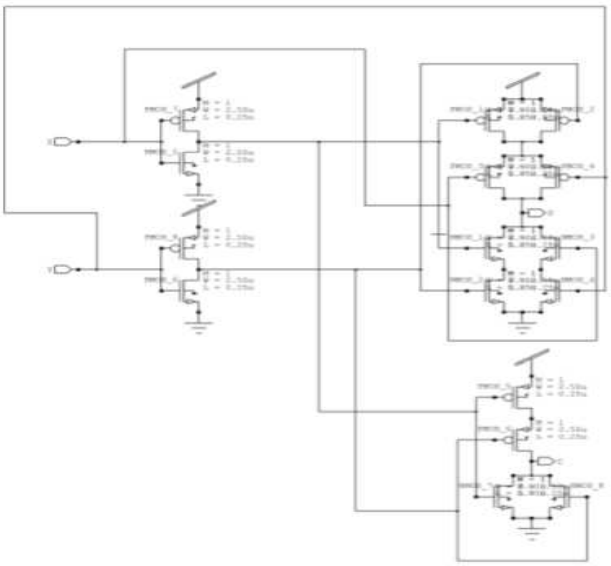
A.1 2(AR):



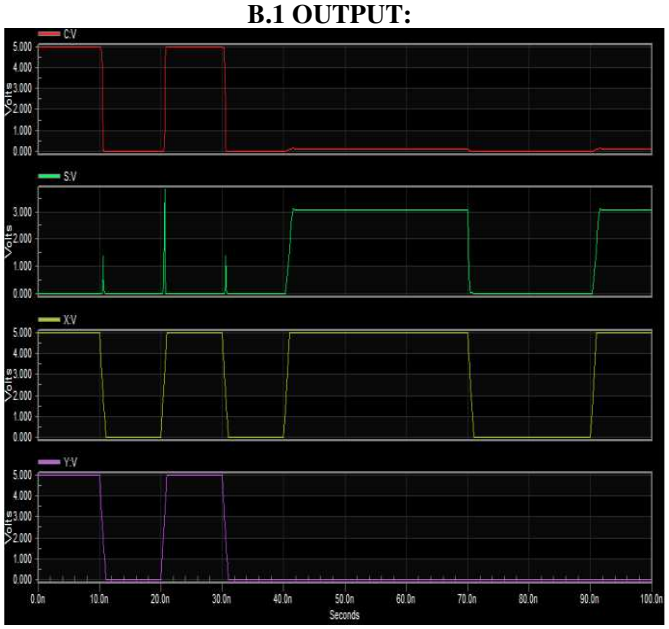
A.3 N2AR:



A.2 NA2R:



B.1 OUTPUT:



V. CONCLUSION:

It has been observed from the simulation results that performance of adder architectures varies with operand combinations. The output of the four different designs of Half adders are same. The current fabrication size of Half adder is 125nm.If the fabrication size reduced to less than 100nm, the Half adder performance varies and can be absorbed using static (CMOS) technology. From this research the (CMOS) can be achieved by operating0 point within 0.9v.This research is very useful and more advantageous in microprocessor industries.

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