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"Investigations on Control Strategies of Multilevel Inverters to Reudced CMV and THD for Improved Power Quality"

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Abstract— **Multilevel inverter has become most popular over the years in the area of high power medium voltage energy control. With the recent advancement in Power semiconductor switches, multilevel inverter fed induction motor drives are extensively used in industries. Common mode voltage (CMV) is the voltage measure between star point of load and system ground. CMV is produced in inverter causes current to flow through bearings which may cause premature failure of the motor bearings. This paper presents the reduction of CMV in Diode Clamped multilevel Inverter using multicarrier SPWM technique. A MATLAB Simulation of diode clamped multilevel inverter is presented by applying different multicarrier modulation techniques. CMV and THD are investigated**

Index Terms— **CMV, THD, Multicarrier Sinusoidal pulse width modulation, DCMLI**

I. INTRODUCTION

Power Electronics deals with efficient and Effective use of electrical energy with the help of power semiconductor switches on-off control. The number of industry applications in which induction motors are fed by voltage source inverters is growing fast. Motor bearing life has been from six to ten years if distortion less ac power supply is given to the motor. Now a days motor bearing fails early than its life. This is because of high frequency bearing currents through motor bearing. Modern variable speed drives operates at high switching frequencies. In PWM switched 3-phase power supply to VSD, dc voltage is converted to ac voltage, but neutral point voltage is not zero. This voltage between system ground and load neutral is common mode voltage. Current flowing due to this voltage finds return path through motor bearing, shaft and inverter. Changes in inverter output voltage gives current pulses through bearings. This high frequency bearing currents may damage bearing [11].Magnitude of this current can be reduced by reducing CMV.

Common mode voltage can be reduced in multilevel inverters by applying proper modulation technique in multilevel inverter. Multilevel inverters invented with the specific aim of overcoming the voltage limit capability of power devices. 3-level NPC has highest converter efficiency among available solutions and it is preferred choice in many industrial MV applications [5]

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II. CONTROL AND MODULATION TECHNIQUES

Multicarrier PWM strategy is widely adopted modulation strategy for MLI, several triangular carrier signals are compared with one sinusoidal modulating signal. (m-1) triangular carriers are required to produce m-level output. All carriers have the same peak to peak amplitude Ac and same frequency fc. The reference waveform has peak to peak amplitude of Am and a frequency fm. Each carrier signal is compared with reference, and when reference signal is greater than carrier signal, pulse is generated. 1. Phase Disposition SPWM strategy (PD SPWM). In this modulation strategy, (m-1) carriers are compared with modulating sine wave of frequency fm to generate m level output. All the (m-1) carrier signals are of same frequency fc and same amplitude Ac and all are in same phase [7]. Fig 3(a) shows PD modulation strategy generated SPWM pulses. The SPWM pulses for five levels DCMLI is generated in MATLAB simulation as shown in waveform. Fundamental frequency and %THD of line voltage for different modulation indices for conventional PWM Strategy as shown in able 1.

Table 1 Fundamental frequency and %THD of line voltage

Different Modulation Schemes	Fundamental Frequency-Line Voltage	Total Harmonic Distortion (THD) Line voltage
PDPWM	348.1	16.95
VAPDPWM	377.0	17.39
PODPWM	377.0	20.16
VAPODPWM	367.1	20.15
APODPWM	346.9	25.15
VAAPODPWM	376.9	21.23
VFPWM	346.8	18.78
COPWM-A	364.1	21.21
COPWM-B	364.1	23.87

A. Diode clamped multilevel inverter

Diode Clamped Multilevel Inverter is the most widely used topology which gives the step in the output voltage with the used of clamping diode. Decrease in the power device voltage stress is the main concept of DCMLI with use of diode. An typical n-level DCMLI requires (n-1) voltage source, 2(n-1) switching device, (n-1)(n-2) diode [4],[5]. With the increase in the level of Diode Clamped Inverter the output voltage waveform improved and came closer to the sinusoidal

waveform with decrease in CMV and THD [1],[3].The Diode Clamped Multilevel Inverter structure is most suitable for high and medium voltage motor drives. The main drawback of DCMLI is that it uses an additional requirement of a clamping diode but this drawback can be overcome with the DCMLI advantages [4]. Magnitude of the harmonic is lowered and at low switching frequency THD is less, low switching losses, low dv/dt rating, reduced CMV. The fig1 (a), fig1 (b) and fig1 (c) shows structure of 3-level, 5-level, 7-level and 9-level Diode clamped multilevel inverter with its step output in figures respectively.

B. Basic Diode clamped multilevel inverter model (B-DCMLI)

Values of various parameters used in this model are given in table 1, Fig. 1 show schematic diagram of basic diode clamped multilevel inverter. These figures are the basic diode clamped or neutral point clamped topology. DC link capacitor is used to divide the input DC voltage and provide clamping arrangement to multi-stair waveform.

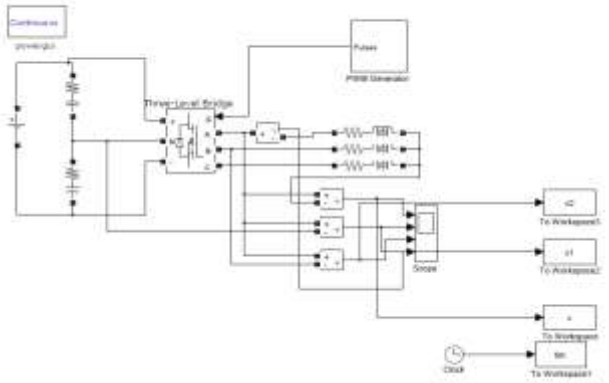

Figure 1 Model of Basic Model of DCMLI

Table 2 Simulation Parameters for B-DCMLI

Parameters	Value
Amplitude	100 volts
Resistance	0.01 Ω
Capacitor	2200e-6 F
Amplitude Modulation Index M	0.95
Snubber resistance, Snubber capacitance	Rs=1e5, Cs=inf.
Frequency modulation index	M_f=50
Load	R = 15 Ω, L = 5e-3H

C. Diode clamped multilevel inverter (DCMLI)

Values of various parameters used in this model are given in table. 2 Fig. 2 show schematic diagram of basic Diode Clamped Multilevel Inverter. In 3-level DCMLI total of 8 IGBTs, 7 clamping diodes and 4 V_{cc} supply. The DC voltage source may be a battery or rectified voltage through uncontrolled/controlled bridge rectifier known as passive/active front end converter, respectively. To obtain $+V_{dc/2}$ voltage at inverter pole.

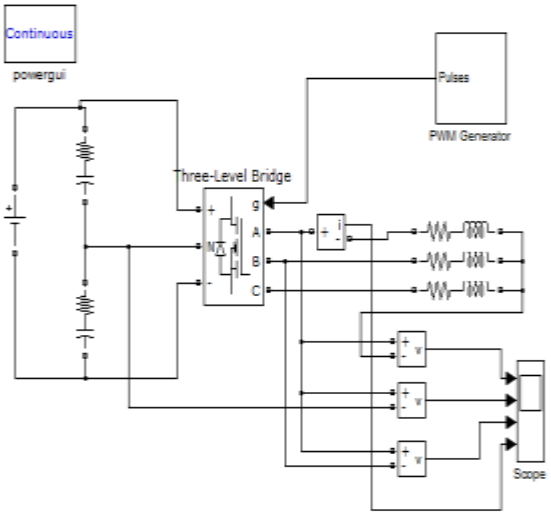

Figure 2 Model of Diode Clamped Multilevel Inverter

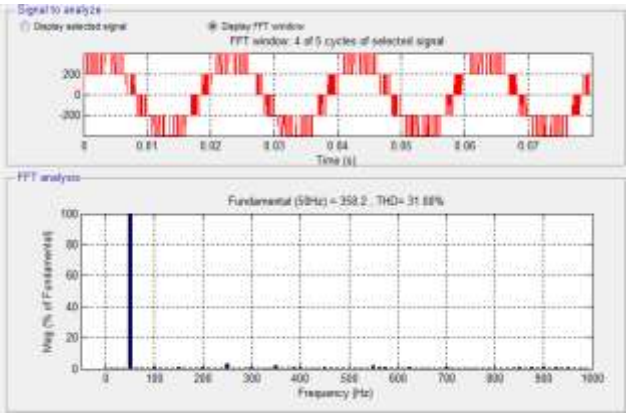

Figure 3 Simulation result of Diode clamped multilevel inverter (DCMLI) V line

Table 3 Simulation Parameters DCMLI

Parameters	Value
Amplitude	125 volts
Resistance, Inductance	0.001 Ω, 0H
Nominal frequency, Active power	F_n = 50 Hz, P = 100 W
forward voltage, fall time, tail time	V_f=1 V, T_f=1e-6 S, T_t=2e-6 S
Snubber resistance, Snubber capacitance	Rs=500 Ω, Cs = 250e-9 F
On resistance value	R_{on}=0.001 Ω
Forward voltage, Initial current	V_f=0.8 V, I_c=0 A

D. Five level diode clamped multilevel inverter SPWM

Values of various parameters used in this model are given in table 3. Nine different Modulation schemes is used. Figure 5 show schematic diagram of five levels diode clamped Multilevel Inverter. Shows the output line voltage whose amplitude is around 199.5 volts which is close to 200 volts, the harmonic profile of the output line voltage while Figure 5 shows the output phase voltage waveform whose amplitude is around 199.5 volts which is close to 200 volts. The output phase voltage in figure 5 refer to the line voltage, phase voltage and there harmonic profile respectively.

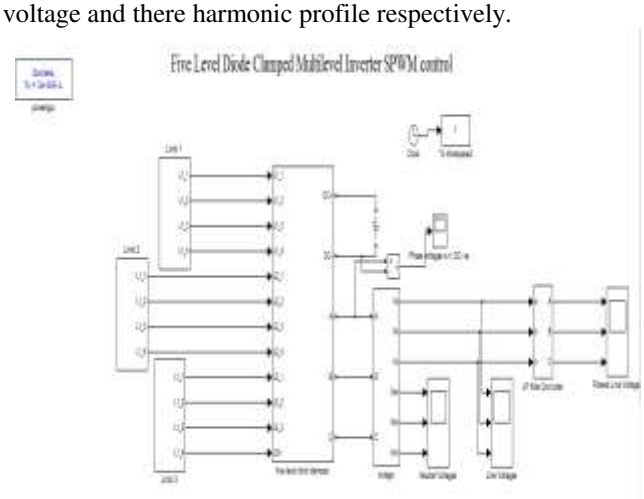

Figure 4 Model of Five Level Diode Clamped Multilevel Inverter SPWM

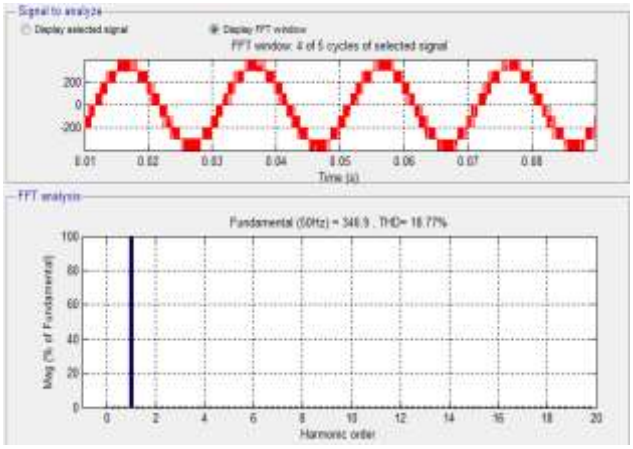

Figure 5. Simulation result of Five Level Diode Clamped Multilevel Inverter SPWM V line

Table 4 Simulation Parameters for Five level Multilevel Inverter

Parameters	Value
R_{int} and $R_{snubber}$ of MOSFET/diode	0.1 Ω, 10^5Ω
V_{dc}	125 volts
Load	R = 50 Ω, L = 10 Mh
Modulation Index M	0.85
$f_{carrier}$	1 kHz
f_{ref}	50 Hz
Capacitance and R_{ESR} of dc-link and floating capacitors	4000µF, 200 Mω

E. Simulation model of seven level multilevel inverters

Values of various parameters used in this model are given in table. 4 figure 7 show schematic diagram of Seven level multilevel inverter. Figure 8 Shows the output phase voltage Va= 304.7 and V Line= 526.7 . And THD are **5.73%, 5.01%.**

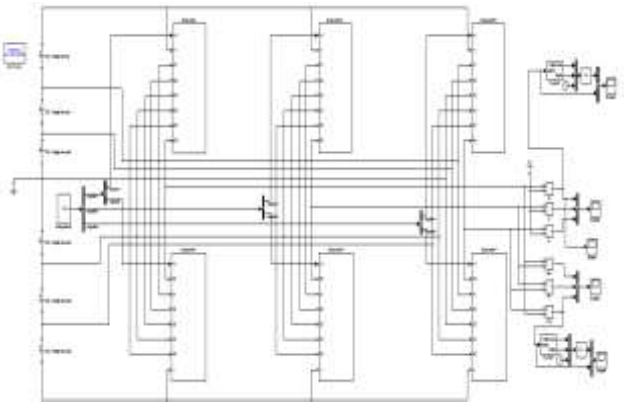

Figure 6 Model of Seven Level Diode Clamped Multilevel Inverter SPWM

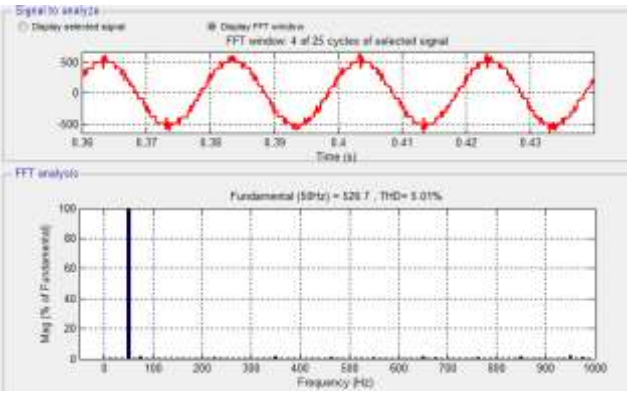

Figure 7 Simulation Result of Seven Level Diode Clamped Multilevel Inverter SPWM
(V Line)

F. Simulation model of nine level Multilevel Inverters

Values of various parameters used in this model are given in table 5 Fig. 8 show schematic diagram of nine level multilevel inverter. Figure 9 and 10 Shows the output phase voltage Va= 402.7 and line voltage V Line= 694.8. And THD are **4.40% , 4.03%.**

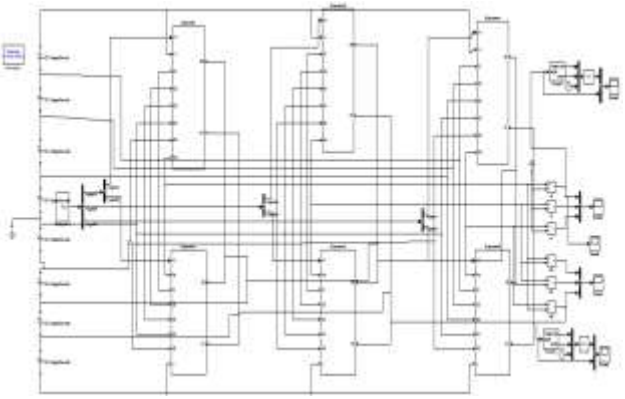

Figure 8 Model of Nine Level Diode Clamped Multilevel Inverter SPWM

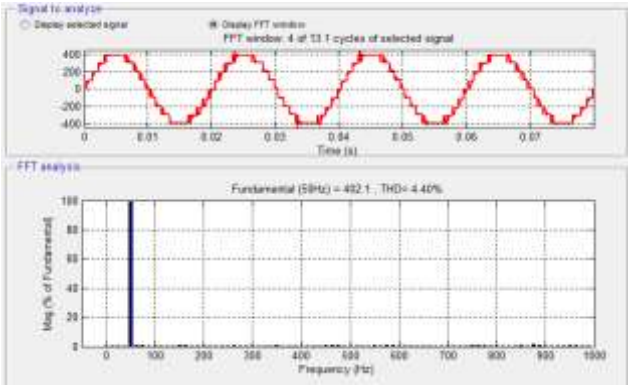

Figure 9 Simulation result of nine level multilevel inverter (V phase)

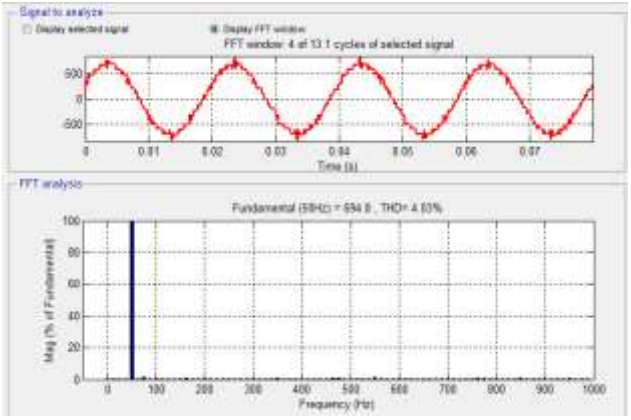

Figure 10 Simulation result of nine level multilevel inverter (V Line)

Table 5 Comparisons table of deferent multilevel inverters

S.No	Multilevel of Inverters	Fundamental Frequency(50 Hz)	THD %
1	Basic DCMLI	Va= 206.00	31.13%
2	Five level MLI	Vph= 200.2 VLin= 346.9 Vneutral= 200	26.53% 18.72% 18.71%
3	Seven Level MLI	Va= 304.7 VLine= 526.7	5.73% 5.01%
4	Nine Level MLI	Va= 402.7 VLine= 694.8	4.40% 4.03%

III. CONCLUSION

3-level, 5-level and 7-level and 9-level Diode clamped multilevel inverter is simulated in MATLAB Simulink. The simulation output gives a conclusion that by employing different multicarrier based SPWM technique we can reduce the CMV or eliminate the CMV. By applying multicarrier based POD SPWM strategy, CMV obtained is less as compared to PD and APOD strategy and improved Power Quality

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