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Evaluation of Reversible Computing Using Ancient Methods

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Abstract— **Due to the ever growing demand for high speed processors advancement in the technology regards to speed is the peak area of interest. The first word strike when the parameter speed is concerned is multiplication. Since multiplication is an important fundamental function in all mathematical computations it dominates the execution time of most throughput determination & CPU cycle time of a system. In a typical processor, Multiplication is one of the basic arithmetic operations and it requires substantially more hardware resources and processing time than addition and subtraction. In fact, 8.72% of all the instruction in typical processing units is multipliers. In computers, a typical central processing unit devotes a considerable amount of processing time in implementing arithmetic operations, particularly multiplication operations. In this project, the comparative study of different multipliers is done for low power requirement and high speed, also gives information of "Urdhva Tiryakbhyam" algorithm of Ancient Indian Vedic Mathematics which is utilized for multiplication to improve the speed, area parameters of multipliers. In this paper, we develop a novel architecture to perform high speed multiplication using ancient Vedic mathematics. One of the most efficient sutra in Vedic mathematics named as Urdhva Triyakbhyam strikes a difference in the actual multiplication process. In current scenario, the reversible logic design attracting more interest due to its low power consumption. Reversible logic is very important in low-power circuit design. The important reversible gates used for reversible logic synthesis are Feynman Gate, Fredkin gate, toffoli gate, New Gate sayem gate and peres gate etc. In this paper, evaluating various bits of reversible Vedic multiplier circuits based on Urdhava Triyakbhyam Sutras (Vertical and Crosswise Algorithm) to optimize the area, Quantum cost and garbage output of the Vedic multiplier circuits. This multiplier can be efficiently adopted in designing Fast Fourier Transforms (FFTs) Filters and other applications of DSP like imaging, software defined radios, wireless communications. The Total Reversible Logic Implementation Cost (TRLIC) is used as an aid to evaluate the proposed design. The proposed algorithm is developed using Verilog HDL. Implementation has been done using Xilinx14.6.**

Index Terms— **Quantum Computing, Reversible Logic Gate, Vedic Mathematics, Urdhava Triyakbhyam, Optimized Design, Total Reversible Logic Implementation Cost (TRLIC)**

I. INTRODUCTION

With the advancement in the VLSI technology, there is an ever increasing quench for portable and embedded Digital Signal Processing (DSP) systems. DSP is omnipresent in almost every engineering discipline. Faster additions and multiplications are the order of the day. Multiplication is the most basic and frequently used operations in a CPU. Multiplication is an operation of scaling one number by another. Multiplication operations also form the basis for other complex operations such as convolution, Discrete Fourier Transform, Fast Fourier Transforms, etc. With ever increasing need for faster clock frequency it becomes imperative to have faster arithmetic unit. Therefore, DSP engineers are constantly looking for new algorithms and hardware to implement them. Vedic mathematics can be aptly employed here to perform multiplication. Vedic Mathematics is one of the most ancient methodologies used by the Aryans in order to perform mathematical calculations. This consists of algorithms that can boil down large arithmetic operations to simple mind calculations. The above said advantage stems from the fact that Vedic mathematics approach is totally different and considered very close to the way a human mind works. The efforts put by Jagadguru Swami Sri Bharati Krishna Tirtha Maharaja to introduce Vedic Mathematics to the commoners as well as streamline Vedic Algorithms into 16 categories or Sutras needs to be acknowledged and appreciated. The Urdhva Tiryakbhayam is one such multiplication algorithm which is well known for its efficiency in reducing the calculations involved. Another important area which any DSP engineer has to concentrate is the power dissipation, the first one being speed. There is always a tradeoff between the power dissipated and speed of operation. The reversible computation is one such field that assures zero power dissipation. Thus during the design of any reversible circuit the delay is the only criteria that has to be taken care of. In a reversible Urdhva Tiryakbhayam Multiplier had been proposed. The proposed multipliers are designed using Vedic mathematics and the evaluation of these multipliers having different bits by the use of reversible logic gates to optimize the area, Quantum cost and garbage output of the multipliers. The methodology started with the conventional logic design implementation of a 2x2 Urdhva Tiryakbhayam multiplier using the irreversible logic gates. In the four expressions for the output bits are derived and are used to obtain the reversible implementation. The overall performance of the UT multiplier is scaled up by optimizing each individual unit in terms of quantum cost, garbage outputs etc. The design expressions can be logically modified so as to optimize the design. The reversible logic circuit with multiple numbers of same inputs is not advisable. Finally the designed structure is simulated and the result is obtained which gives the report objective.

II. VEDIC MATHEMATICS

Vedic Mathematics is the name given to the ancient system of Indian Mathematics which was rediscovered from the Vedas between 1911 and 1918 by Sri Bharati Krishna Tirthaji (1884-1960). According to his research all of mathematics is

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based on sixteen Sutras, or word-formulae. For example, 'Vertically and crosswise` is one of these Sutras. These formulae describe the way the mind naturally works and are therefore a great help in directing the student to the appropriate method of solution. [1]

The term 'Veda' means storehouse of knowledge. Vedic Mathematics is an ancient form of mathematics reconstructed from ancient Indian scriptures referred to as Vedas. It is based on 16 sutras which transact different branches of mathematics like algebra, geometry, arithmetic. These Sutras along with their brief meanings are enlisted below alphabetically.

1. (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.
2. Chalana-Kalanabyham – Differences and Similarities.
3. Ekadhikina Purvena – By one more than the previous One.
4. Ekanyunena Purvena – By one less than the previous one.
5. Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
6. Gunitasamuchyah – The product of the sum is equal to the sum of the product.
7. Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.
8. Paraavartya Yojayet – Transpose and adjust.
9. Puranapuranabyham – By the completion or non-completion.
10. Sankalana- vyavakalanabhyam – By addition and by subtraction.
11. Shesanyankena Charamena – The remainders by the last digit.
12. Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.
13. Sopaantyadvayamantyam – The ultimate and twice the penultimate.
14. Urdhva-tiryagbhyam – Vertically and crosswise.
15. Vyashtisamanstih – Part and Whole.
16. Yaavadunam – Whatever the extent of its Deficiency. [1][2]

III. URDHVA TRIYAKBHYAM SUTRA

The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. [1][2]

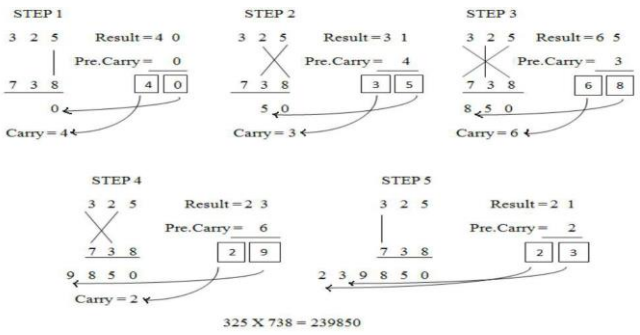

Figure1: Multiplication of two decimal numbers

To illustrate this multiplication scheme, for example, the multiplication of two decimal numbers (325 * 738). Line diagram for the multiplication is shown in Fig.2. The digits on the both sides of the line are multiplied and added with the carry from the previous step. This generates one of the bits of the result and a carry. This carry is added in the next step and hence the process goes on. To make the methodology more clear, an alternate illustration is given with the help of line diagrams in figure.4 where the dots represent bit „0" or „1". [12] algorithm for 4×4 bit multiplication Using Urdhva Triyakbhyam

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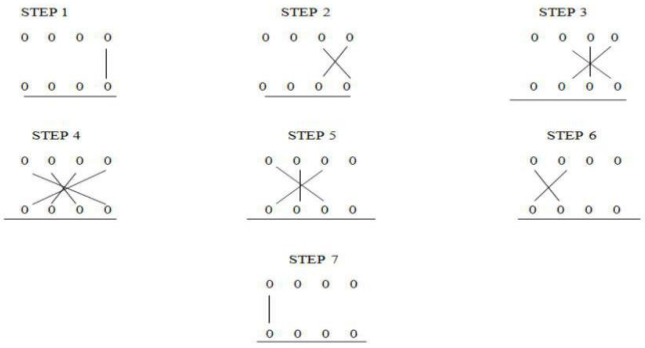

Figure 2: Line diagram for multiplication of two 4- bit numbers

Firstly, least significant bits are multiplied which gives the least significant bit of the product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the product and the carry is added in the output of next stage sum obtained by the crosswise and vertical multiplication and addition of three bits of the two numbers from least significant position.

IV. REVERSIBLE LOGIC GATES IN USE

Feynman Gate:

Fig.3 shows a 2*2 Feynman gate. The input vector is I (A, B) and the output vector is O (P, Q). The outputs are defined by P=A, Q=A□B. Quantum cost of a Feynman gate is 1. [6]

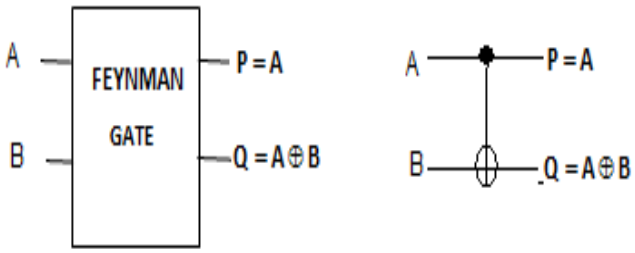

Fig 3: Feynman gate

Double Feynman Gate (F2G):

Fig.4 shows a 3*3 Double Feynman gate. The input vector is I (A, B, C) and the output vector is O (P, Q, and R). The outputs are defined by P = A, Q=A□B, R=A□C. Quantum cost of double Feynman gate is 2. [9]

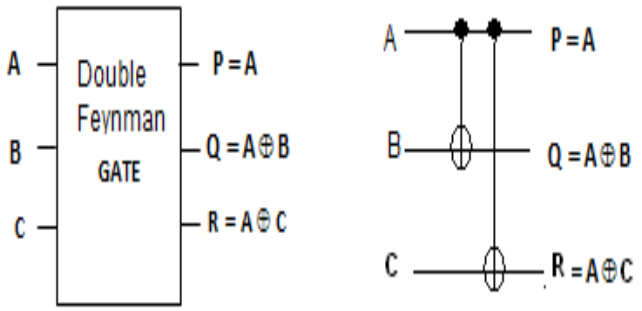

Fig 4: Double Feynman gate

Toffoli Gate:

Fig 5 shows a 3*3 Toffoli gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5. [9]

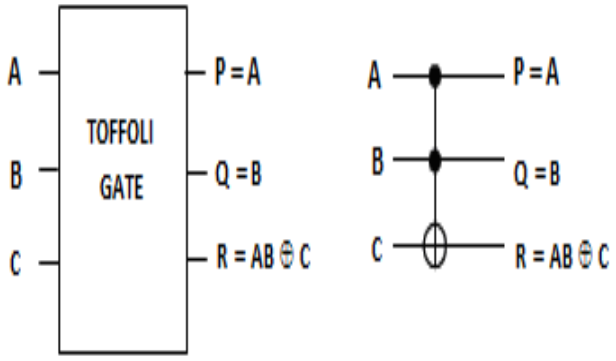

Fig 5: Toffoli gate

Fredkin Gate:

Fig 6 shows a 3*3 Fredkin gate [4]. The input vector is I (A, B, C) and the output vector is O (P, Q, and R). The output is defined by P=A, Q=A′B⊕AC and R=A′C⊕AB. Quantum cost of a Fredkin gate is 5. [6]

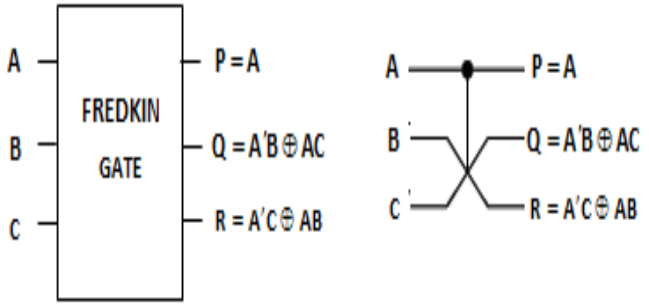

Fig 6: 3*3 Fredkin gate

BVF Gate:

Fig.7 shows a 4 * 4 BVF gate. This is a reversible double XOR gate and can be used for duplication of the required inputs to meet the fan-out requirements. The input vector is I(A,B,C,D) , the output vector is O(P,Q,R,S) and the output is defined by P = A, Q = A⊕B, R = C and S = C⊕D. Quantum cost of a BVF gate is 2. In the proposed design this gate is used to copy the operand bits and it is shown that the number of gates required to copy is reduced by 50% with same quantum cost. [6]

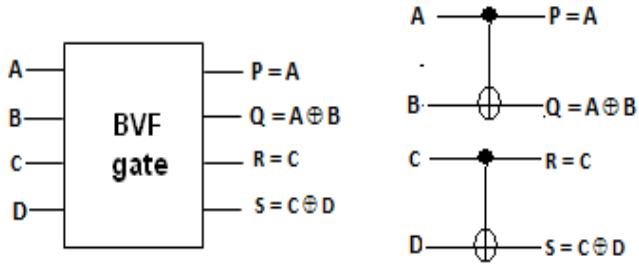

Fig 7: BVF gate

The existing 4*4 gates namely MKG, TSG, HNG and PFAG can be individually used as an adder. Of all this HNG gate has least hardware complexity. It is shown that using the proposed DPG gate the quantum cost of the multiplier is kept to the minimum value and at the same time it is more flexible as it can be used either as a half adder or as a full adder.

Peres Gate:

Fig 8 shows a 3*3 Peres gate [10]. The input vector is I (A, B, C) and the output vector is O (P, Q, and R). The output is defined by P = A, Q = A⊕B and R=AB⊕C. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost. [6]

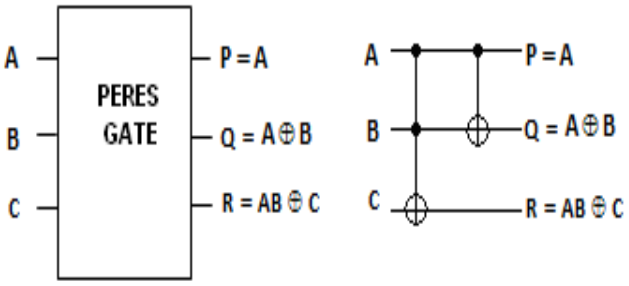

Fig 8: Peres gate

A full-adder using two Peres gates is as shown in fig 9. The quantum realization of this shows that its quantum cost is 8 two Peres gates are used.

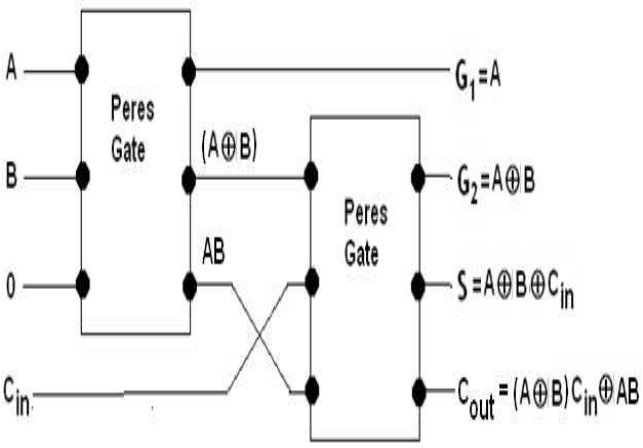

Fig 9: Full adder using two Peres gates

A single 4*4 reversible gate called PFAG gate with quantum cost of 8 is used to realize the multiplier. In the Proposed multiplier a reversible adder gate called Double Peres Gate (DPG) is used and its quantum cost is 6.

Double Peres Gate:

Fig 10 shows a Double Peres Gate. The inputs and outputs are as shown in Table-1.The full adder using DPG is obtained with C=0 and D= Cin and its quantum cost is calculated to be equal to 6 from its quantum realization shown in fig.9.

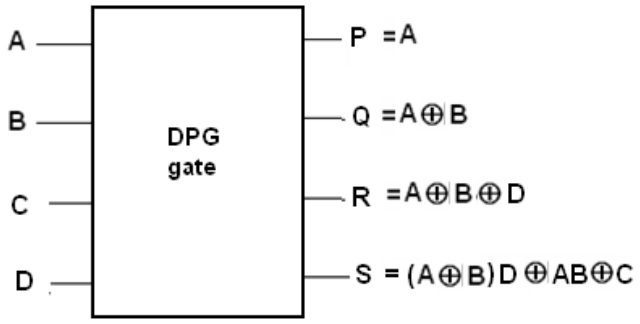

Fig 10: DPG gate

2x2 Vedic Multiplier:

It has two 2-bit binary number A and B as input and 4-bit number S as output. Where A =a1a0 and B =b1b0 let output is S =s3s2s1s0 and c1and c2 are the carry generated in s1 and the s2, which is shown in the figure.1. Output is given as:

s0 = a0b0;
s1 = a1b0 + a0b1;
s2 = c1 + a1b1;
s3 =c2;

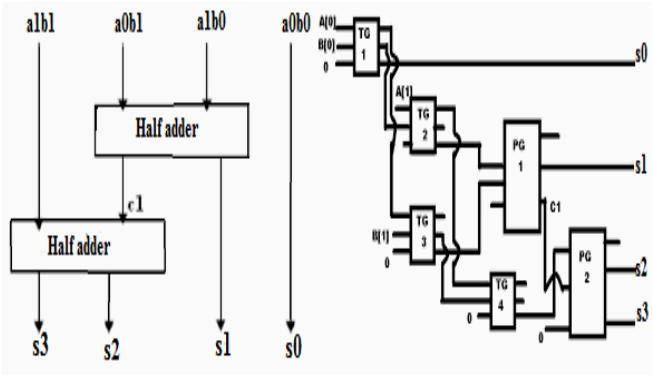

Fig.11. 2x2 Vedic multiplier using TG and PG gates

There are four TG and two PG gates are used in realizing 2x2 Vedic multiplier. Total six reversible gates are used in this implementation. Number of constants and number of garbage values is six and quantum cost is 28. This implementation looks same as array and booth multiplier, So 2-bit Vedic multiplier does not give much advantage over other methods but 4x4 and 8x8 does.

4x4 Vedic Multiplier:

The 4x4 bit binary Vedic multiplier can be implemented using four 2x2 bit Vedic multiplier units. Let 4x4 multiplications having input A= a3a2a1a0 and B= b3b2b1b0 and the output the multiplication result is F= F7F6F5F4 F3F2F1F0. Using the fundamentals of UT sutra, taking two bits at a time and using four 2x2 multipliers, 4-bit binary multiplication will be calculated. The 4x4 vedic multiplier is shown in the figure.12.

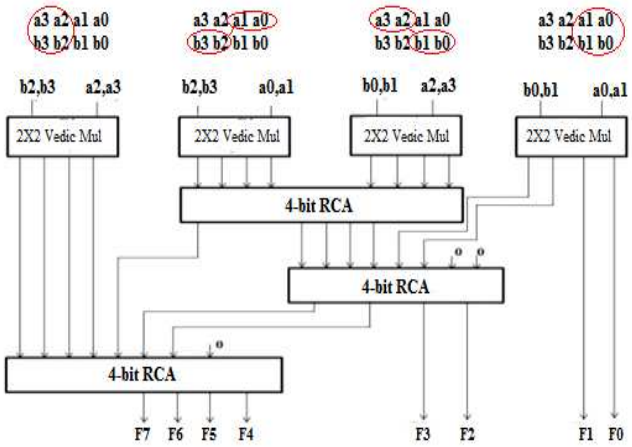

Fig.12. 4x4 Vedic multiplier

This design consists of four 2x2 vedic multiplier, and three 4-bit ripple carry adder circuit. This purposed design reduces the delay because it has property of concurrency. It has quantum cost of 144, constant input is 32 and garbage output is 44. The proposed 4x4 Vedic multiplier has less quantum cost, constant inputs and garbage value. This design is used for implementing the proposed 8x8 Vedic multiplier.

8x8 Vedic Multiplier

The proposed 8x8 Vedic multiplier block diagram is shown in the figure 13. It is easily implanted using four 4x4 vedic multiplier and three 8-bit ripple carry adder. This makes the design of this proposed 8x8 multiplier very simple and efficient compare to the array and booth type multipliers. All the multipliers are made using PG and TG reversible gates. And RCA is design using HNG gates. So the designs are reversible in nature. It has quantum cost of 720.

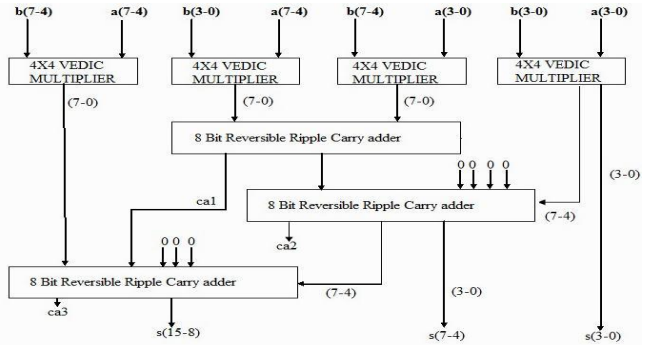

Fig.13. Proposed 8x8 Vedic multiplier

8-bit Reversible Ripple Carry Adder:

Reversible adder is proposed using HNG gate. In HNG gate if fourth input, D is made constant zero and inputs is given through A and B and carry to third input C then it act as reversible one bit full adder and output is taken from R and S respectively. The proposed 8-bit reversible adder is form using HNG gate having two 8-bit inputs and a carry which is propagate from the list significant bit (LSB) to most significant bit (MSB) also known as ripple carry adder. The size of the reversible ripple carry adder is very small and it is very simple to design, so normally ripple carry adders are

used for cascading. Each HNG gate act as one bit full adder so total eight HNG gates are required to build 8-bit ripple carry adder. Output is represented as S0-S7 and „g" is the garbage. The 4 bit ripple carry adder is made with same HNG gate. In proposed adder total 16 garbage values are produced and having quantum cost of 48. The proposed reversible 8-bit ripple carry adder is shown in the figure 14.

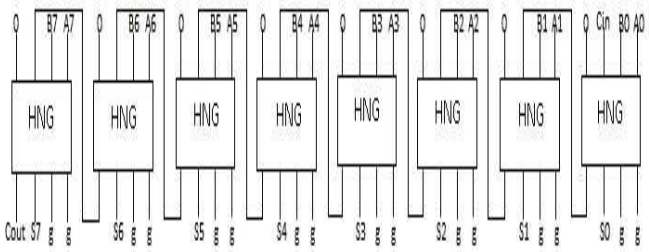

Fig.14. Proposed 8-Bit RCA using HNG Gate.

Design of 32X32 Reversible Multiplier:

The Reversible 32X32 Urdva Tiryakbhayam Multiplier design emanates from the 16X16 multiplier. The block diagram of 32X32Vedic multiplier is presented in the Fig.16. It consists of four 16X16 multipliers each of which produce 32 bits as inputs; 16 bits from the multiplicand and 16 bits from the multiplier. The lower 16 bits of the output of the first 16X16 multiplier are entrapped as the lowest 16 bits of the final result of multiplication. 16 zeros are concatenated with the upper 16 bits and give as input to the 32 bit ripple carry adder. The center two multipliers which produce 32 bits each as a outputs and these outputs are concatenated to 32 bit ripple carry adder, which produces an output of 33 bit, these 33 bits is given as input to 33 bit ripple carry adder which produces 34 bits, of these LSB 16 bits is taken as output. Then remaining 18 bits is given to 32 bit ripple carry adder, which is having 32 bits as input from the last multiplier, then 32 ripple carry adder generates 32 bits as output.

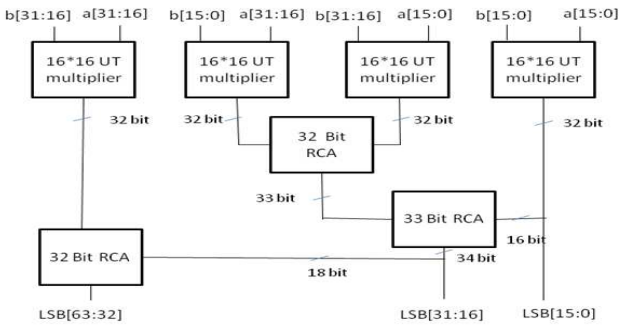

Fig.15. Block Diagram of 32X32 UT multiplier.

V. CONCLUSION

The Urdhva Tiryakbhayam Vedic Multiplier is evaluated using reversible logic gates. Firstly a basic 2x2 UT multiplier is designed. This design stems from the conventional logic implementation. After this, the 2x2 UT multiplier block is cascaded to obtain the 4x4 multiplier. The 4x4 UT multiplier block is cascaded to obtain the 8x8 multiplier. The 8x8 UT multiplier block is cascaded to obtain the 16x16 multiplier. The 16x16 UT multiplier block is cascaded to obtain the 32x32 multiplier. The ripple carry adders which were required for adding the partial products were constructed using HNG gates.4 bit Vedic multiplier designed and get simulation and synthesis waveforms using Xilinx 13.2.

FUTURE SCOPE

Will help in reducing power consumption,
Will help in reducing propagation delay.
Will help in reducing area of digital circuits.
Will help in high speed operation of ALU & CPU.

REFERENCES

[1]Swami Bharati Krsna Tirtha, Vedic Mathematics. Delhi: Motilal Banarsidass publishers 1965
[2] Vedic Mathematics: http://www.hinduism.co.za/vedic.html.
[3] R. Landauer,"Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, 5, pp.183-191, 1961.
[4]C.H. Bennett, "Logical reversibility of Computation", IBM J. Research and Development, pp.525-532, November 1973.
[5]R. Feynman, "Quantum Mechanical Computers," Optics News, Vol.11, pp. 11–20, 1985.
[6]A. Peres, Reversible logic and quantum computers, Phys. Rev. A 32 (1985) 3266–3276.
[7]E. Fredkin and T. Toffoli,"Conservative Logic", Int'l J. Theoretical Physics Vol 21, pp.219-253, 1982.
[8]Shivangi S Jain, Vandana Jagtap, Vedic Mathematics in Computer: A Survey, International Journal of Computer Science and Information Technologies, Vol. 5 (6), 2014, 7458-7459
[9]Prashant.R.Yelekar, Prof. Sujata.S.Chiwande, Introduction to reversible logic gates and its applications, 2nd National Conference on Information and Communication Technology (NCICT) 2011 Proceedings published in International Journal of Computer Applications® (IJCA)
[10] P.koti laksmi, B santosh kumar, Prof.Rameshwar Rao, IMPLEMENTATION OF VEDIC MULTIPLIER USING REVERSIBLE GATES, David C. Wyld et al. (Eds) : ACITY, DPPR, VLSI, WiMNET, AIAA, CNDC – 2015
[11] Rakshith Saligram, Rakshith T.R Optimized Reversible Vedic Multipliers for High Speed Low Power Operations, 978-1-4673-5758-6/13/$31.00 © 2013 IEEE Conference on Information and Communication Technologies (ICT 2013)
[12] SHAIK WAHID BASHA, H SOMA SHEKAR, Design and Implementation of Reversible Vedic Multiplier for High Speed Low Power Operations, International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE) Volume 3, Issue 12, December 2014
[13] GOPATHOTI VINOD KUMAR, KANDULA RAVI KUMAR, ANANDA BABU BATTU Optimized Reversible Vedic Multipliers for High Speed Low Power Operations, International Journal of VLSI System Design and Communication Systems Volume.02, IssueNo.11, December-2014, Pages: 1134-1139
[14] T.Nagaveer, M.Neelima, VNM Brahmanandam K Performance Analysis of Vedic Multiplier Using Reversible Logic in Spartan 6, International Journal of Research in Computer and Communication Technology, Vol 3, Issue 10, October - 2014
[15] Boddu Suresh, B.Venkateswara Reddy DESIGN AND IMPLEMENTATION OF EFFICIENT HIGH SPEED VEDIC MULTIPLIER USING REVERSIBLE GATES, International Journal of Advance Research In Science And Engineering IJARSE, Vol. No.3, Issue No.7, July 2014 ISSN-2319-8354(E).
[16] Parameswara reddy, B. Balasubbanna Optimized Reversible Vedic multipliers for High Speed Low Power Operations, International Journal of Research (IJR) e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 07, July 2015
[17] Shifana Parween, S. Murugeswari , PG Scholar, M.E (VLSI Design), Sri Ramanujar Engineering College, Chennai, India, Design of High Speed, Area Efficient, Low Power Vedic Multiplier using Reversible Logic Gate, International Journal of Emerging Technology and Advanced Engineering (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 4, Issue 2, February 2014)
[18] G Ganesh Kumarand V Charishma, Design of high speed vedic multiplier using vedic mathematics techniques, Itn'l J. of Scientific and Research Publications, Vol. 2 Issue 3 March 2012

[19] Rakshith Saligram and Rakshith T.R. "Design of Reversible Multipliers for linear filtering Applications in DSP" VLSICS, Vol No (6), Dec-12
[20] H. R. Bhagyalakshmi, M. K. Venkatesha, "An Improved Design of a Multiplier using Reversible Logic Gates," IJEST, Vol. 2, No.
[21] G.Ganesh Kumar and V.Charishma , Design of High Speed Vedic Multiplier using Vedic Mathematics Techniques SVEC College Tirupati , International Journal of Scientific and Research Publications, Volume 2, Issue 3, March 2012 ISSN 2250-3153
[22] Swaroop A. Gandewar and Mamta Sarde, Design of vedic multiplier for complex numbers for enhanced computation using VHDL, International Journal of Industrial Electronics and Electrical Engineering, ISSN: 2347-6982 Volume-2, Issue-5, May-2014
[23] Gaurav Sharma, Arjun Singh Chauhan, Himanshu Joshi and Satish Kumar Alaria, Delay Comparison of 4 by 4 Vedic Multiplier based on Different Adder Architectures using VHDL, International Journal of IT, Engineering and Applied Sciences Research (IJIEASR) ISSN: 2319-4413 Volume 2, No. 6, June 2013
[24] Kavita, Umesh Goyal, Performance Analysis of Various Vedic Techniques for Multiplication International Journal of Engineering Trends and Technology- Volume4Issue3- 2013
[25] R.K. Bathija, R.S. Meena, S. Sarkar, Low Power High Speed 16x16 bit Multiplier using Vedic Mathematics, International Journal of Computer Applications (0975 – 8887) Volume 59– No.6, December 2012
[26] Mr. Dharmendra Madke, Assoc.Prof. Sameena Zafar, M.Tech Scholar Associate Professor (EC Department) P.C.S.T,(R.G.P.V) Bhopal (M.P.), Review Paper on High Speed Karatsuba Multiplier and Vedic Mathematics Techniques, International Journal of Advanced Research in Computer Science and Software Engineering, Volume 3, Issue 12, December 2013.
[27] Harsimranjit Kaur, Dr. Neelam Rup Prakash , Compressor Based Area-Efficient Low-Power 8x8 Vedic Multiplier, Nidhi Pokhriyal et al Int. Journal of Engineering Research and Applications ISSN : 2248-9622, Vol. 3, Issue 6, Nov-Dec 2013
[28] Arushi Somani, Dheeraj Jain, Sanjay Jaiswal, Kumkum Verma, Compare Vedic Multipliers with Conventional Hierarchical array of array multiplier, International Journal of Computer Technology and Electronics Engineering (IJCTEE) Volume 2
[29] Manjeet Singh Sankhwar, Rajesh Khatri Design of High Speed Low Power Multiplier Using Nikhilam Sutra with Help of Reversible Logic International Journal Of Modern Engineering Research (IJMER) ISSN: 2249–6645 | www.ijmer.com | Vol. 4 | Iss. 1 | Jan. 2014
[30] G. Sree Lakshmi, Dr.Kaleem Fatima and Dr.B.K. Madhavi Design and Implementation of Vedic Multiplier using Reversible Logic Proceedings of Third National Conference on Latest Trends in Signal Processing, VLSI and Embedded Systems ISBN 978-93-83459-63-6