International Journal of Engineering and Technical Research (IJETR)
ISSN: 2321-0869 (O) 2454-4698 (P) Volume-8, Issue-01, January 2018

Power Analysis of an Approximate adders under various interpolation factors for DSP Applications

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Abstract— **Energy-efficiency is a critical concern for many systems, ranging from the Internet of things objects and mobile devices to high-performance computers. Moreover, after 40 years of prosperity, Moore's law is starting to show its economic and technical limits. Many circuits are noticed that they are over-engineered and many are error-resilient applications or require less precision than offered by the existing hardware, approximate computing has emerged as a potential solution to pursue improvements of digital circuits. In this regard, a technique to systematically tradeoff accuracy in exchange for an area, power, and delay savings in digital circuits is proposed.**

Index Terms—**Approximate Adders, CMOS, Low Power, Pass Transistor**

I. INTRODUCTION

Improving energy efficiency of modern computing systems is the main challenge in today's digital design. Computing capabilities of mobile devices such as smartphones has grown exponentially in the past decades. Additionally, the number of Internet of things devices is expected to reach 21 billion by 2020. The latter not only requires to operate for several years without user intervention, but will also produce a gigantic amount of data that will have to be processed in data centers which are extremely power hungry and need complex cooling systems.

In the past four decades, technology scaling has been leading integrated circuits' advancement. Unfortunately, the growing complexity of deeply scaled technology combined with increasing process-voltage–temperature variations and the poor scaling of Vth, Moore's law is starting to show its limits. Nonetheless, approximate computing which can be applied through different abstraction layers ranging from technology, hardware design, up to algorithm or software level is a potential solution to pursue the challenge of computing advancement and overcome the physical and economical limitations encountered with technology scaling.

Approximate computing has become a promising technique to reduce the power, area and delay constraints in VLSI design, albeit at the expense of a loss in computational accuracy. This technique is applicable to error-tolerant applications such as multimedia, mining and recognition. Generally, there are two methodologies for reducing accuracy by approximation.

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The first methodology uses a voltage-over-scaling (VOS) technique for CMOS circuits to save power, while also introducing errors into the circuit. The second methodology is based on redesigning a logic circuit into an approximate version.

The main objective of the "Low Power Approximate Adders For General Computing Using Differential Transmission Gate" is to noticing that many circuits are over-engineered and that many applications are error-resilient or require less precision than offered by the existing hardware, approximate computing has emerged as a potential solution to pursue improvements of digital circuits.

II. EXISTING SYSTEM

Approximate computing allows remarkable power and energy savings by relaxing computation accuracy while achieving an acceptable processing quality. The key observation is that many applications, such as digital signal processing and neuromorphic systems, have inherent error resilience and hence 100% precision in computation is not required. Particularly, the core of many DSP and neuromorphic10 applications lies in processing specific kernel functions. For example, spiking neural networks heavily perform the leaky integrate-and-fire (LIF) operation to mimic neuron behaviour. Obviously, adders are one primary component for building these arithmetic kernel functions. In addition, comparators are indispensable to determine firing activities in the LIF operation of digital neurons. To this end, it is particularly attractive to design approximate arithmetic units for considerable energy saving in neuromorphic computing.

The approximate adder of leverages a limited number of less significant input bits for carry speculation to increase the overall speed. The critical drawback of this approach is the use of a considerable number of carry generators, which gives rise to large area and high power dissipation. The error tolerant adder I and the lower part OR adder are split into an accurate part for higher output bits and an inaccurate part, which utilizes a modified XOR or an OR function to approximately compute the remaining lower bits.

A. Approximate Adder - Mux Selection Logic

The block diagram of the existing approximate n-bit adder, which is divided into several k-bit sized blocks. Each block contains a k-bit SA and a k-bit sub-carry generator (SCG), which create a partial summation and partial carry-out signal, respectively.

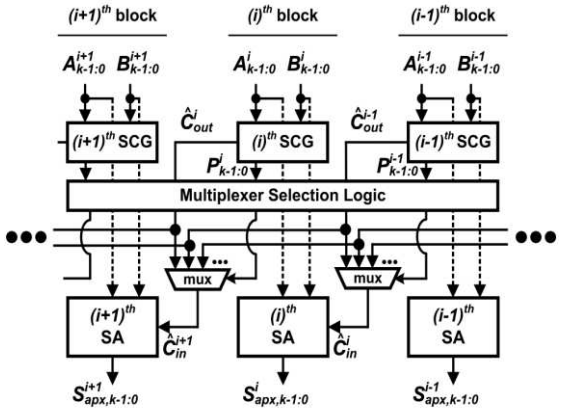


Fig.1 Approximate Adder Using Mux Selection Logic

Note that the SAs can be implemented by any accurate adders, such as ripple-carry adder (RCA) and carry-look ahead adder (CLA). At the beginning of an addition operation, all the SCGs simultaneously create the partial carry-out signals (. . ., Ci+1, Ci , Ci−1, . . .) using only their k-bit inputs.

B. Approximate Comparator - Mux Selection Logic

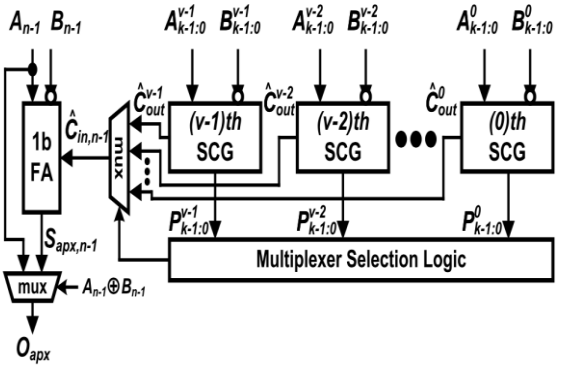


Fig.2 Approximate Comparator Using Mux Selection Logic

This block diagram of the proposed approximate comparator. The n-bit comparator consists of a 1-bit full adder (FA) and v (≥2) k-bit SCGs that are identical to the ones in the proposed adder. It is worth noting that the proposed approximate comparator exploits only kv + 1 MSBs of the n-bit inputs, resulting in area and power reductions. Importantly, the input B is inverted to achieve subtraction operation. Since implementing two's complement necessitates an additional increment or, we employ one's complement to further reduce area and energy with sacrificing an error rate, but still achieving a very low error rate. The FA generates the sign bit Sapx,n−1 (MSB output) of the subtraction between the two inputs by leveraging the speculated carry-in signal Cin,n−1 and the MSB of the two inputs. The speculated carry-in signal is obtained in the same parallel way by the v SCGs and multiplexer selection logic.

The carry prediction is incorrect if all the propagate signals of more than v consecutive blocks are true and a carry is generated in the preceding block, making a carry chain of a length greater than kv. Assuming that the adder inputs A and B are bitwise independent, then the propagate and generate signals are bitwise independent as well.

When the two inputs have the different signs (i.e., An−1 ⊕ Bn−1 = 1), the comparison result is readily obtained by the input MSB without the FA. Therefore, the output multiplexer selects the MSB of the input An−1 if the signs of two inputs are different from each other, otherwise, it chooses the FA output S_{apx}, n−1. The comparator fails when the signs of the inputs are the same and the carry prediction for the FA is incorrect. The carry speculation is incorrect when all the propagate signals in the v SCGs used for carry prediction are true and a carry generated from the n − kv − 1 least significant bits (LSBs). It is important to note that, weshouldconsiderallthepropagatesignalsofthen−kv−1LSBs are true since the proposed comparator adopts one's complement, instead of two's complement, for the subtraction. We assume that the inputs A and B are bitwise independent. Then, the event of the carry prediction error for the FA is given by

$$E^{i}_{\text{cin}} = P^{i-1}_{k-1:0} P^{i-2}_{k-1:0} \cdots P^{i-v}_{k-1:0} G^{i-v-1}_{k-1:0} . \quad (1)$$

C. Approximate Comparator

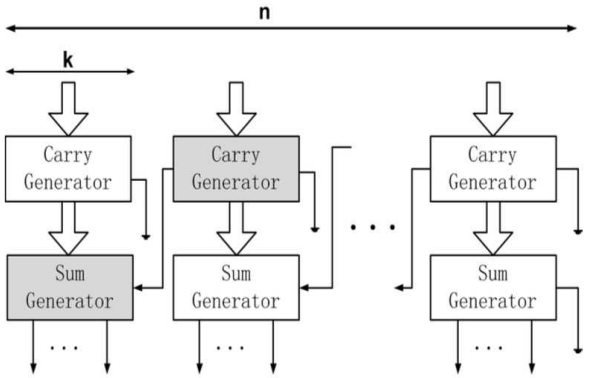


Fig.3 Approximate Comparator Using Combinational Logic

A dynamic segmentation and error compensation scheme is presented in for an approximate adder design. This approximate adder consists of several sub-adders of different sizes divided from an n-bit adder; each of the sub- adders operates in parallel and has a truncated carry input. For convenience, but with no loss in correctness, sub-adders of equal size are considered in this manuscript. More over the error compensation part is neglected because the focus of this manuscript is on analyzing the approximate operation.

The existing comparator fails when the signs of the inputs are the same and the carry prediction for the FA is incorrect. The carry speculation is incorrect when all the propagate signals in the v SCGs used for carry prediction are true and a carry generated from the $n - kv - 1$ least significant bits (LSBs). It is important to note that, we should consider all the propagate signals of the $n-kv-1$LSBs are true since the proposed comparator adopts one's complement, instead of two's complement, for the subtraction. We assume that the inputs A and B are bitwise independent. Then, the event of the carry prediction error for the FA is given by

$$E_{\text{cin},n-1} = P^{v-1}_{k-1:0} P^{v-2}_{k-1:0} \cdots P^{0}_{k-1:0} \left(G_{n-kv-2:0} + P_{n-kv-2:0}\right). \quad (2)$$

III. PROPOSED SYSTEM

Pass Transistor Logic

Pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage.

Each transistor in series is less saturated at its output than at its input. If several devices are chained in series in a logic path, a conventionally constructed gate may be required to restore the signal voltage to the full value. By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply rails, so logic voltage levels in a sequential chain do not decrease. Simulation of circuits may be required to ensure adequate performance.

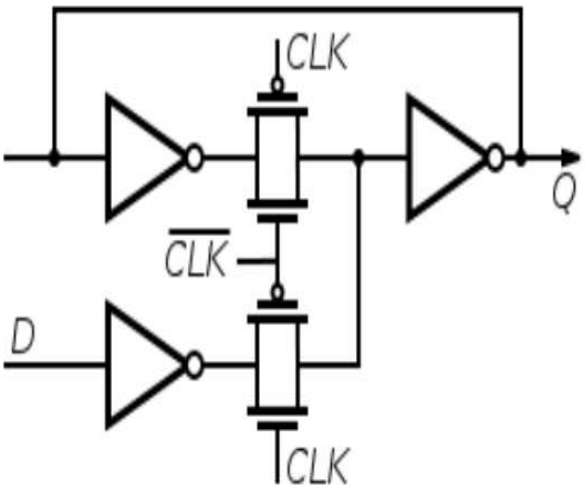


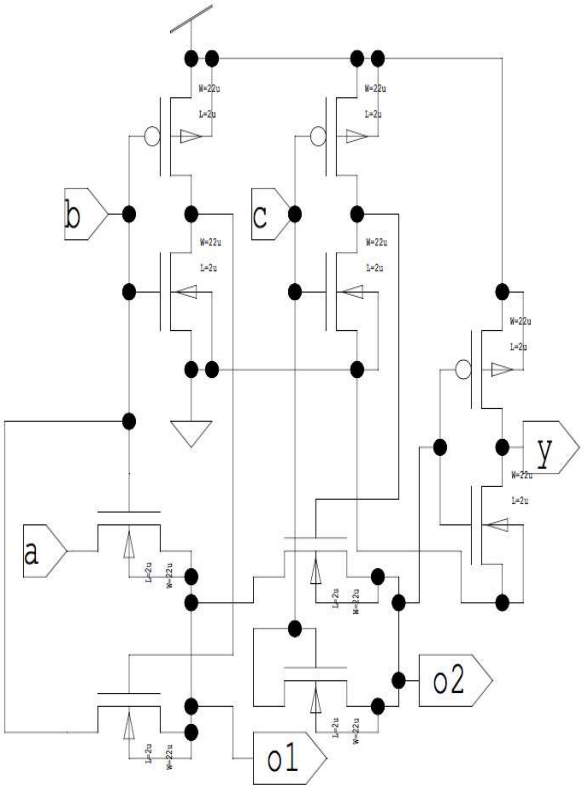
Fig.4 Complementary Pass Transistor

Complementary pass transistor logic or "Differential pass transistor logic" refers to a logic family which is designed for certain advantage. It is common to use this logic family for multiplexers and latches. CPL uses series transistors to select between possible inverted output values of the logic, the output of which drives an inverter The CMOS transmission gates consist of nMOS and pMOS transistor connected in parallel.

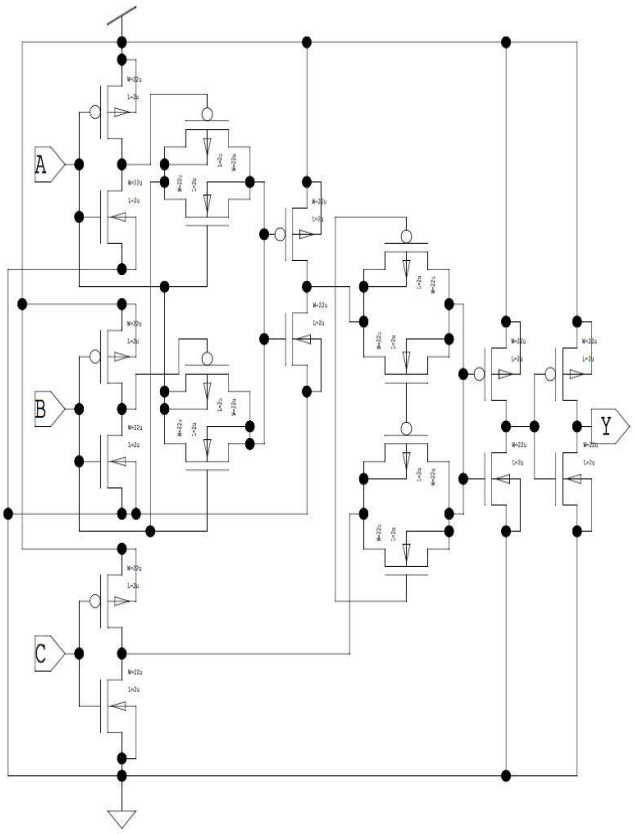
Transmission Gate

Just like transistor, a faucet is connected to a source, the faucet drains in a sink, and the flow of water through the faucet is controlled by a gate (the knob). If the faucet knob (gate) is turned ON water flows from the source to the sink, otherwise if the faucet knob (gate) is turned OFF no water flows. Using transistors as building blocks, we can build larger circuits that perform interesting (logical) operations.

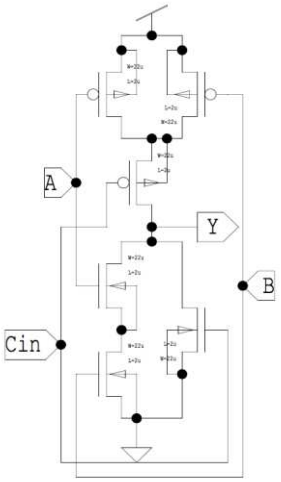
A. Approximate Adders Using Pass Transistor Logic



B. Approximate Adders Using Transmission Gates

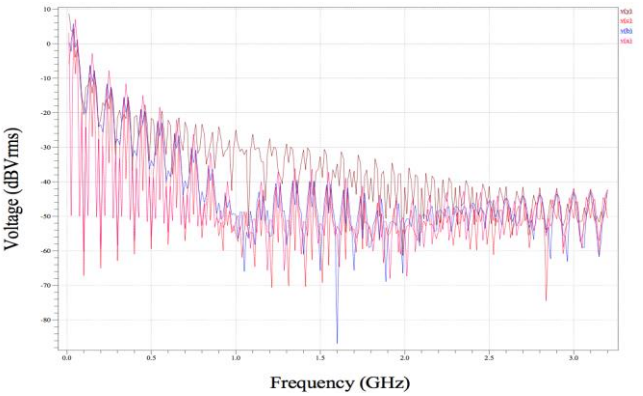


C. Approximate Adders Using CMOS Logic

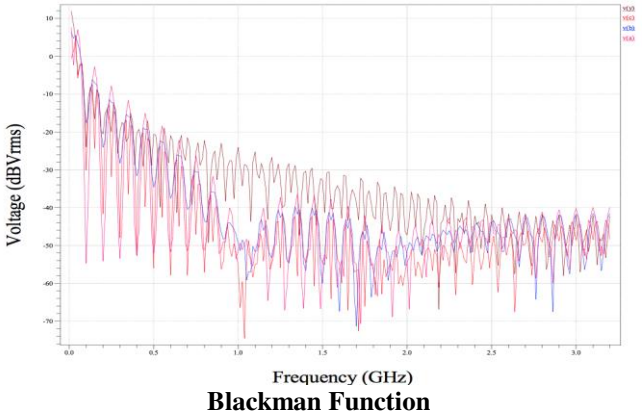


IV. RESULT

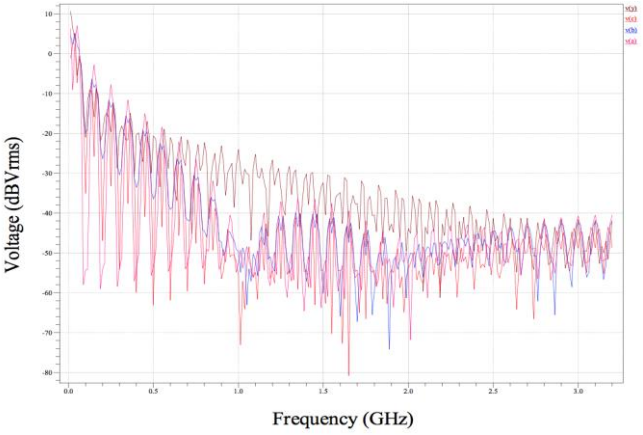
Bartlett Function



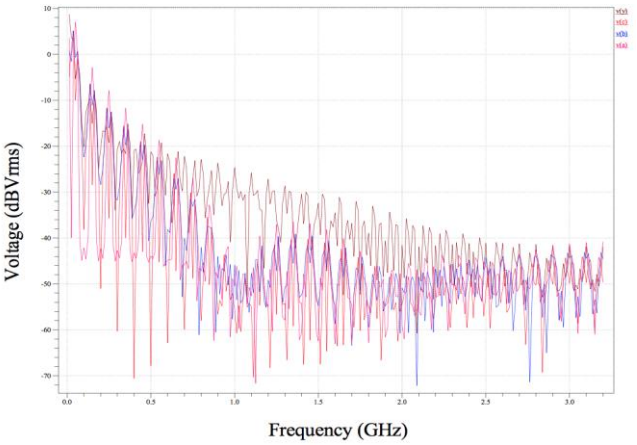
Blackman Harris Function



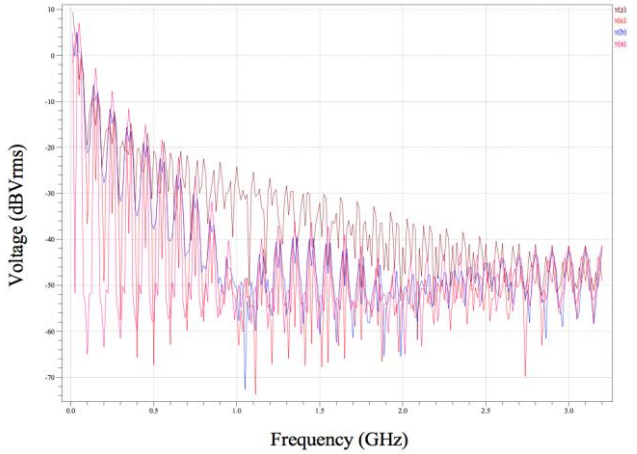
Blackman Function



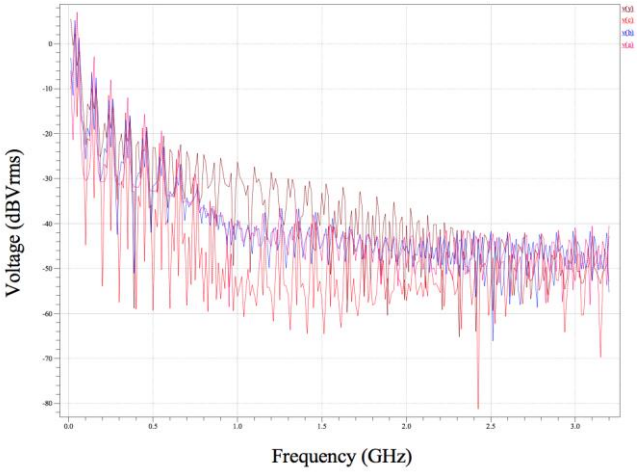
Hamming Function



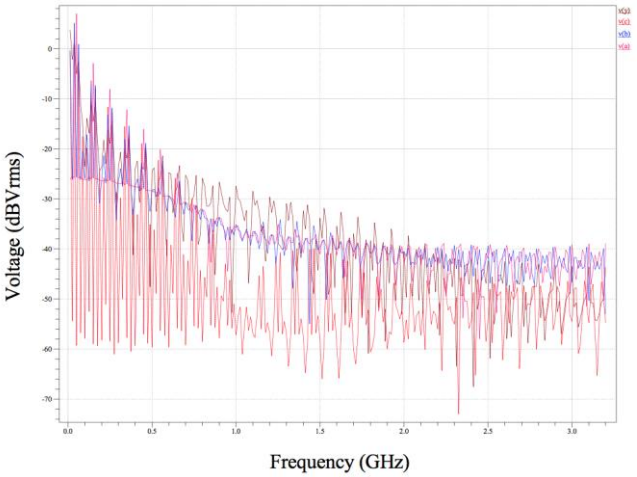
Hanning Function



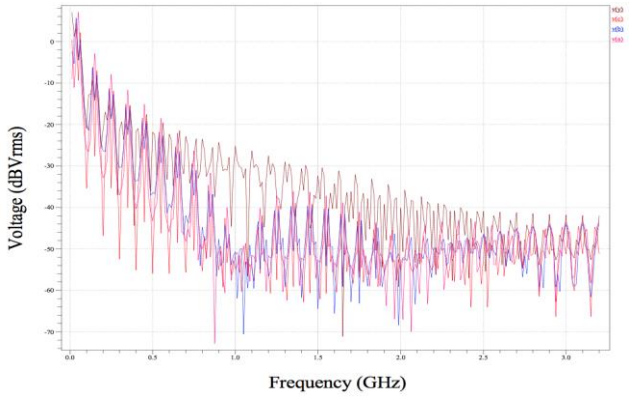
Kaiser Bassel Function



Rectangular Function



Welch Function




```
Power Results
v1 from time 0 to 8e-008
Average power consumed -> 2.612743e+000
watts Max power 2.794875e-002 at time
7.1e-008
Min power 4.172384e-007 at time 0
```

V. CONCLUSION

Approximate adder and comparator designs to considerably reduce energy consumption with a very moderate error rate has been presented for energy efficient neuromorphic VLSI systems. The proposed adder is 2.4× faster and 43% more energy efficient over traditional adders and our comparator achieves up to 71% energy saving over the conventional counterparts.

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