International Journal of Engineering and Technical Research (IJETR)
ISSN: 2321-0869 (O) 2454-4698 (P) Volume-8, Issue-2, February 2018

Static Carry Skip Adder Designed Using 22-nm Strained Silicon CMOS Technology Operating Under Wide Range of Temperatures

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Abstract— **The Technology is rapidly advancing and the world is more electronic today than we have imagined decades ago. This advancement is truly due to small size, low power and high speed. Size reduction is important part for any logic electronic circuitry. This can be only possible by reduction in transistor size.**

Adders are the main building block of any electronic circuit and it is fundamental to build any arithmetic circuit which is used in calculators to super computers. In this paper , we present a static conventional carry skip adder(CSKA) and static proposed carry skip adder(CSKA) using CMOS technology and it is reviewed. We proposed 22-nm Predictive Type Model (PTM) Technology and analyzed static conventional carry skip adder and static proposed carry skip adder . This 22-nm PTM improves the performance and also reduces the area of the adder. Simulation results implies that this 22-nm carry skip adder can be operated under wide range of tempertaures.

Index Terms— **CMOS, Power, Carry skip adder(CSKA), static, high performance, Area reduction**

I. INTRODUCTION

Adders form an integral part of all digital logic circuits and it is mostly used in Arithmetic Logic Unit (ALU) in computers [8]. Whenever we perform a task in computer or compute a multiplication in a computer, adders play an important role in processing in ALU. Adders are everywhere from pocket calculators to super computers and it is the fundamental to any arithmetic logic circuit. So increasing the speed of adders will definitely increase the performance and speed of electronic gadgets, computers, Automatic Teller Machine (ATM). Adders form an integral part of all digital logic circuits and it is mostly used in Arithmetic Logic Unit (ALU) in computers. Adders forms the basis for digital computing of modern world. Adders are the basic digital circuits which perform binary addition and can be used to perform other arithmetic operations. Full Adders are used in parts of processors and also used to calculate the addresses, perform numerical calculations and calculate table indices. Adders are the fundamental part in all modern processors like snapdragon, exynous, Intel Pentium for CPU which consists of Arithmetic Logic Unit. Static circuits have been excellent choice in the design of digital circuits for adders [2]. Static circuits are widely used because of low power consumption compared to dynamic circuits for adders [12]. Static adders are the key part in large industries like Intel due to low power consumption. There are many types of adder families with different delays, power consumptions, and area usages includes ripple carry adder (RCA), carry increment adder (CIA), carry skip adder (CSKA), carry select adder (CSLA) [5] and parallel prefix adders (PPAs) [11]. Ripple carry adder is the simplest adder, but it has longest delay because every sum output needs to wait for the input carry from the previous full adder [10]. The Kogge-Stone parallel prefix adder is one of the fastest structures in addders but have larger area and more power consumption and also it have more structure complexities than CSKA [1]. Conventional Carry Skip Adders are one of the fast and efficient adders unlike parallel prefix adders [15] and it skips or predicts the carry by using multiplexer circuit. Conventional carry skip adders are widely known and almost used everywhere as ripple carry adders faces carry propagation delay issues [9]. Conventional carry skip adders are faster than ripple carry adders. Proposed carry skip adders were introduced for increasing the speed of carry as Conventional carry skip adders has increasing propagation delay as number of bits are increasing in adders. This problem in Conventional Carry Skip adders is avoided by introduction of Proposed Carry Skip adders. The limitation of static circuits for adders lies in the speed compared to dynamic circuits. The Proposed carry skip adders are efficient way to increase the speed of full adders. Proposed Carry Skip adders has a increased area compared to Conventional Carry Adders. The 22 nm CMOS technology helps in increasing the speed and decreasing the area of the carry skip adders. The 22-nm CMOS technology is proven to have low threshold voltage and operate at 0.8V Which is very useful for low power consumption [16]. Decrease in threshold voltage helps in reduction of power consumption since power is directly proportional to threshold voltage. In this paper, the 22-nm CMOS technology is used in Conventional and Proposed Carry Skip Adders. This reduction in transistor size greatly improves the speed and decreases the area of both Conventional and Proposed Carry Skip Adders. Decreasing the area and achieving the better stability is very important. 256 Bit Conventional and proposed carry skip adders are implemented using 22-nm technology using spice tools.

Temperature plays an important role for optimum functioning of Carry Skip adders. Power also plays an significant part for proper functioning as wasted power leads to heat which may result in Circuit malfunctioning. Carry skip adders delay and power are function of temperature and it is necessary to operate it under certain temperatures [3]. Reducing the area of transistor is of primary concern as decrease in size will contribute to decrease in operating voltage of the transistor. Simulation results show the optimum temperature to operate the circuit.

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II. CARRY SKIP ADDER

A. ARCHITECTURE OF CONVENTIONAL CARRY SKIP ADDER

The 4-bit Conventional carry skip adder is implemented using 2:1 multiplexer using static logic is shown in Fig 1. In this architecture, carry skip is achieved by means of exor gates and a multiplexer. This carry skip adder introduces more gates and covers more area than conventional ripple carry adder. However, this adder increases the speed by predicting or skipping the carry. This adder has very lower path delay than conventional ripple carry adder. The focus on carry skip adder arises from maintaining considerably lower area and optimum power consumption. This carry skip adder is implemented by using CMOS logic, which is more reliable in terms of power and operation. The 22nm predictive type model technology further reduces the area, power consumption and operating voltage. The main principle behind this design was to utilize the lower blocks and make them work in parallel with higher blocks.

The output of 2:1 multiplexer is carry output and is computed,

$$Cout = A.Cin + \bar{A}.C3$$

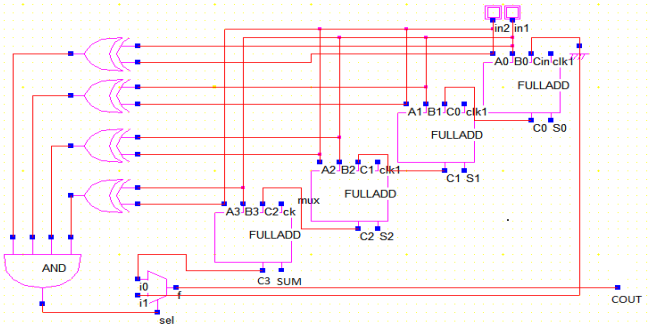

Fig. 1: Logic diagram of Carry Skip Adder.

B. ARCHITECTURE OF PROPOSED CARRY SKIP ADDER

The structure of a 8-bit carry skip adder is implemented using proposed logic is shown in Fig. 2. This proposed logic

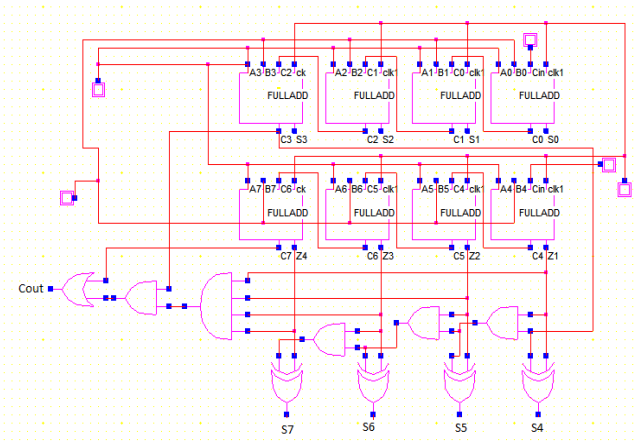

Fig. 2 : Structure of Proposed carry skip adder.

has a larger area compared to conventional carry skip adder. However, this logic increases the speed and has the advantage of lower propagation delay as the conventional carry skip adder suffers propagation delay as the number of one bit full adder increases in the circuitry. The 8-bit Conventional carry skip adder speed is compared with 8-bit Proposed carry skip adder.

By applying concatenation and incrementation techniques, this Proposed carry skip can be implemented for n-bit adder with greater speed enhancement than conventional carry skip adder. In the literature work so far reviewed, more concentration was on speed than power consumption and area. The product of power-delay is lowest among the adder structures and the product of energy-delay is same as that of Kogge-Stone parallel prefix adder. Modification techiques in the proposed carry skip adder provides us the ability to work on simpler carry skip logics by AND-OR compound gate rather than using multiplexer. This further reduces the complexity. In this paper, the proposed carry skip adder is analysed by using 22-nm predictive type technology model. This 22-nm technology reduces the area to greater extent than any other technology in the literature.

III. SIMULATION RESULTS AND COMPARISONS

A. CONVENTIONAL CARRY SKIP ADDER

The 4-bit conventional carry skip adder is simulated using SPICE tools. This is implemented using 22-nm PTM static CMOS technology. The operating voltage is 0.8V. The results are shown in Fig. 3.1, Fig. 3.2, and Fig. 3.3.

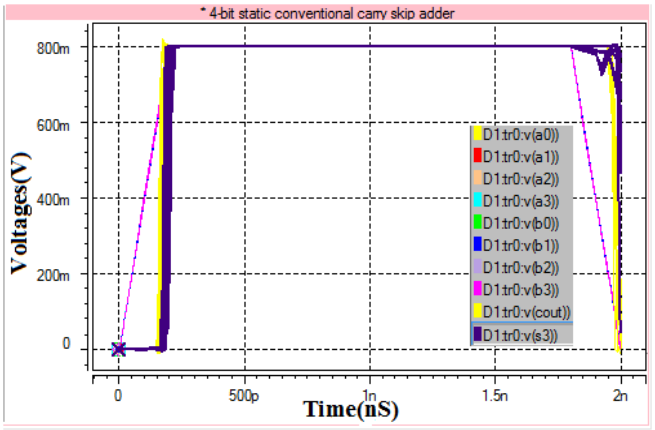

Fig. 3.1: Voltage vs Time characteristics of 4-bit static conventional carry skip adder.

From Fig. 3.1, it is seen that speed of carry is higher than that of sum. The desired speed is achieved and it is shown that it takes only 150pS to rise from logic 0 to 1. The propagation delay is greatly reduced in conventional carry skip adder compared to conventional ripple carry adder. The temperature forms a critical role in the carry skip adder circuitry. As the temperature increases, the usage power of circuit is decreased. This results in wastage of power severely and is noted.

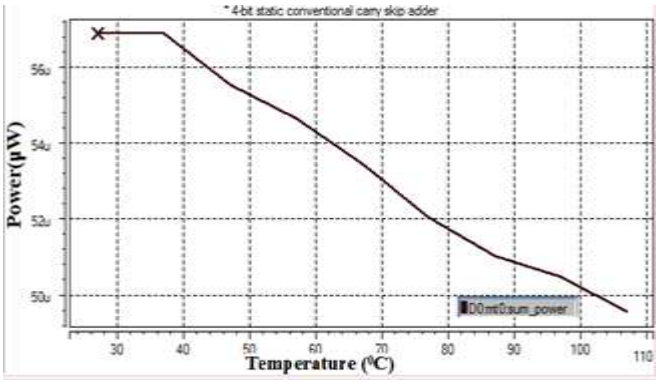

Fig. 3.2: power vs temperature characteristics 4-bit static conventional carry skip adder

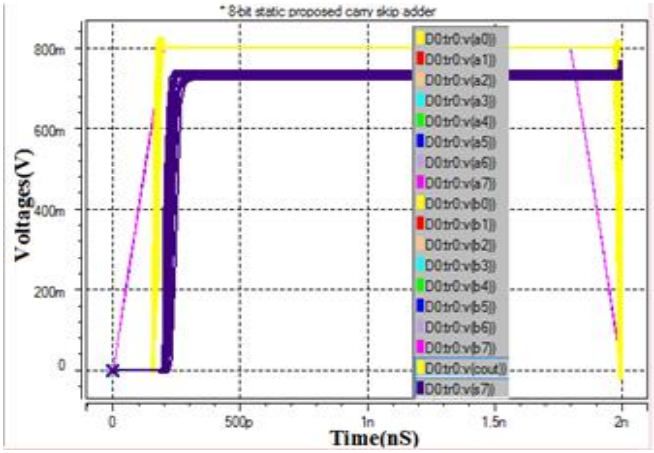

Fig. 3.3: Delay vs temperature characteristics of 4-bit conventional carry skip adder.

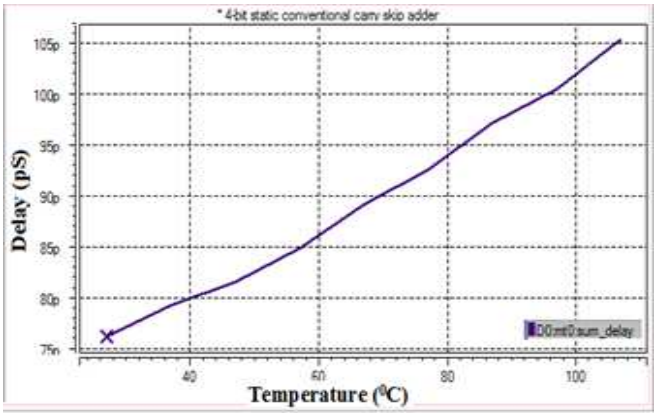

Fig. 3.4: voltage vs time characteristics of 8-bit proposed carry skip adder

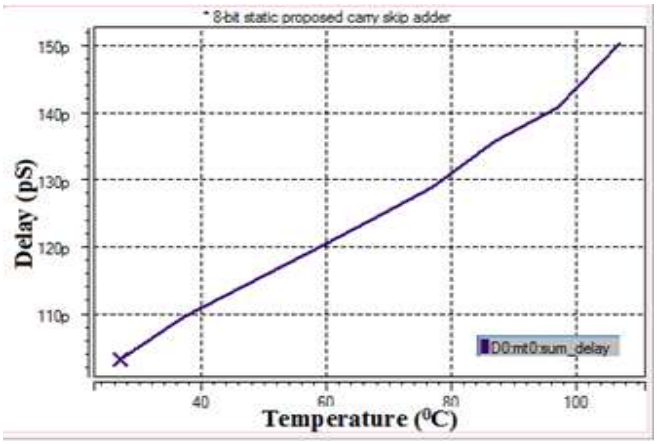

Fig. 3.5: Delay vs temperature characteristics 8-bit proposed carry skip adder

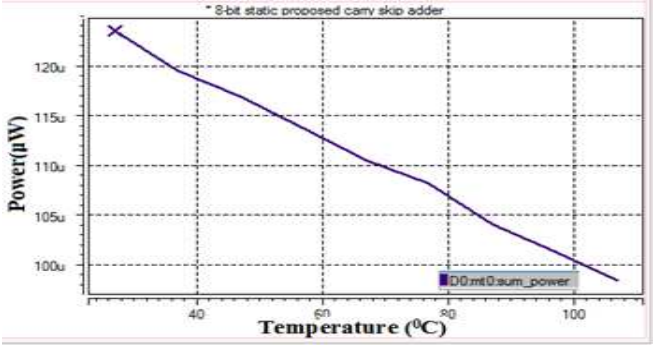

Fig. 3.6: Delay vs temperature characteristics of 8-bit proposed carry skip adder.

From the above results, it is seen that power and delay is inversely proportional to temperature. As the temperature increases, the effective power decreases and more power is wasted as heat. So, it is optimum to operate the circuit from 30^{o} C to 35^{o} C for 4-bit conventional carry skip adder. The delay of 4-bit conventional carry skip adder is minimum around 10^{o}C at 76pS.

The proposed carry skip adder rises from logic 0 to logic 1 in 100pS which is fast compared to conventional carry skip adder architecture which rises from logic 0 to logic 1 in 150pS. Simulation results of voltage vs time graph show that proposed carry skip adder is 33.33% more faster than the conventional carry skip adder which is considerable increase in speed. Even though our proposed carry skip adder has a marginal increase in power consumption of 62.5µW compared to 56.8µW conventional carry skip adder, overall we achieved the lowest power delay product.

B. TABULAR COLUMN:

Type of adders	Static conventional adder		Static proposed adder	
	Delay (pS)	Power (µW)	Delay (pS)	Power (µW)
4BIT	105	56.8	–	–
8BIT	210	113.6	150	124
16BIT	420	227.2	300	248
32BIT	840	454.4	600	496
64BIT	1680	908.8	1200	992
128BIT	3340	1817.6	2400	1984
256BIT	6680	3635.2	4800	3968

Fig. 3.7 22-nm Strained Silicon CMOS technology.

The above table depicts the static conventional and proposed carry skip adder with different bit configuration and delay. Comparing the delay of 8-bit conventional carry skip adder with 8-bit proposed carry skip adder, it is shown that delay of conventional CSKA and proposed CSKA is 210 pS and 150pS. From the delay vs temperature graph from spice tools show that proposed carry skip adder is 28.6% more faster than conventional carry skip adder. Power in the 8 bit conventional carry skip adder is 113.6 µW and Power in the 8-bit proposed carry skip adder is 124 µW. Power consumption in proposed CSKA is 8.4% more than the CSKA. As the number of bits double, delay and power also doubles as seen from the table. Even though the proposed carry skip adder consumes little more power than conventional CSKA, it is more faster which is the main concentration in any adder circuit.

IV. CONCLUSION:

In this paper, conventional carry skip adder and proposed carry skip adder is reviewed. This adders are implemented using 22nm PTM CMOS static technology and the simulation results are obtained. This technology improves the overall performance and considerably speed of the both conventional and proposed carry skip adders. The effect of temperature on power and delay are studied using spice tools.

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