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Single Phase Quasi-Z-Source Based Modified Cascaded Multilevel Inverter with Half-Bridge Cell

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***Abstract*—A new Quasi-Z-Source Modified Cascaded Multilevel Inverter (qZS-MCMLI) with Half-Bridge Cell presents attractive advantages over conventional cascaded MLI with voltage boost ability and reduced switches. The new proposed topology is comprised of cascaded auxiliary units and a full H-bridge inverter, where the auxiliary unit includes half bridge cell with qZS network. With qZS network shoot-through state control, the output voltage amplitude can be boosted, which is not limited to DC source voltage summation similar to conventional cascaded MLI. The performance parameters of qZS-MCMLI with various multicarrier PWM control methods are analysed with simulation results and portrayed here.**

***Index Terms*— Quasi-Z-Source, Cascaded Multilevel Inverter, Half-Bridge Cell, multicarrier PWM, Shoot-through state control.**

I. Introduction

In recent trends, the quasi-Z-source inverter (qZSI) has engrossed ever-increasing applications in renewable energy sources such as Photovoltaic (PV) and wind energy systems [1]. The modern research revealed that the quasi-Z-source concept has been applied to cascaded H-bridge multilevel inverter (CHBMLI) that provides the combined advantages of traditional CHBMLI [2], [3] and qZSI. Quasi-Z-source cascaded multilevel inverter (qZS-CHBMLI) offered numerous merits over traditional CHBMLI in distributed generation applications [4]-[10]. The balanced dc-link voltage and voltage boost capability are the most fruitful advantages of the qZS-CHBMLI. The switching device count increases as the number of levels increases in the conventional CHBMLI that leads to higher switching losses and increased cost for designing the module. Modified Cascaded H-Bridge Multilevel Inverter (M-CHB-MLI) has fascinated extensive interests in recent researches as it leads to reduced number of switches and minimized manufacturing cost. Until now, there is no literature to provide the complete analysis of Quasi-Z-Source Based Modified Cascaded Multilevel Inverter (qZS-MCMLI). The novelty of this paper is to propose the Quasi-Z-Source Modified Cascaded Multilevel Inverter (qZS-MCMLI) with Half-Bridge Cell presenting gorgeous advantages over conventional cascaded MLI with voltage boost ability and reduced number of switches. The qZS-MCMLI has the ability of single stage power conversion with improved reliability and wide voltage control through boost factor and modulation index. The qZS-MCMLI also provides reduced THD and reliability against short-circuits. A multilevel output voltage waveform of the qZS-MCMLI is synthesised by the combination of multicarrier pulse width modulation (MCPWM) technique and simple boost control that launches shoot-through states into the traditional zero states to control the qZS-MCMLI module [11], [12]. The boost control methods uses maximum modulation index to provide output voltage with high voltage gain [13], [14]. In this paper, Phase Disposition Pulse Width Modulation (PD-PWM) control scheme in combination with simple boost control on the proposed topology are analysed.

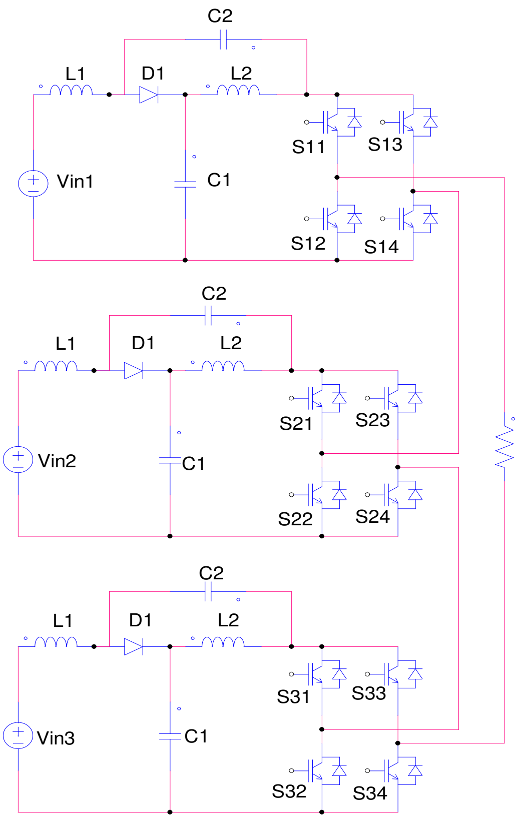

Fig.1. Conventional qZS-CHB-MLI

The conventional qZS-CHB-MLI is shown in Fig 1. It has qZ source network consisting of two inductors (L_1, L_2), capacitors (C_1, C_2) and one diode (D_1). The qZ source network shares the common ground with inverter, and the current drawn by the dc source is continuous.

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II. Proposed Quasi-Z-Source Modified Cascaded Multilevel Inverter

The proposed topology of the qZS-MCMLI with Half-Bridge Cell is depicted as in the Fig.2. The circuit of the qZS-MCMLI is developed such that it can produce multi level outputs with reduced number of semiconductor switches.

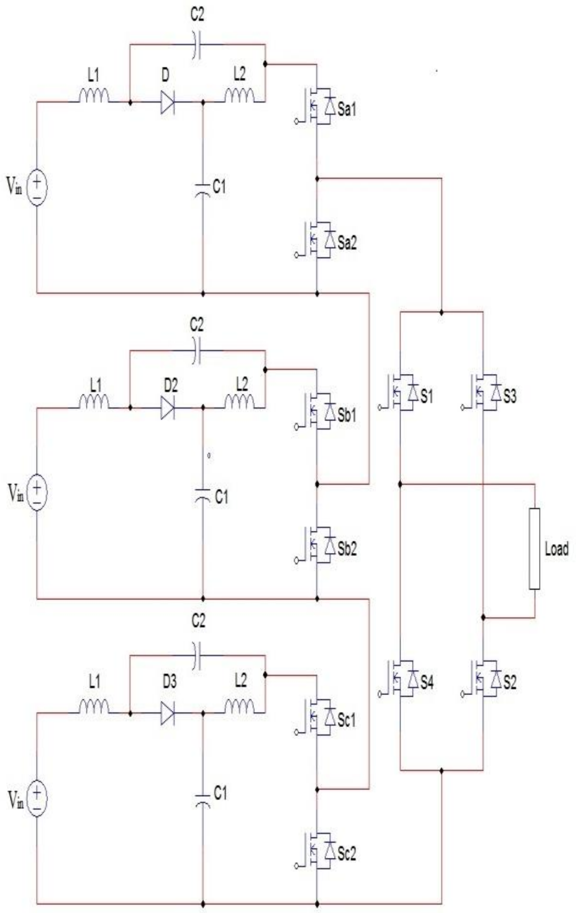

Fig.2. Proposed qZS-MCMLI topology

The topology has cascaded auxiliary units and a full H-bridge inverter, where the auxiliary unit includes half bridge cell with qZS network. The qZS-MCMLI module has a single stage voltage boost and inversion capability. The qZS network in the proposed module can be operated in two modes i.e., non-shoot-through and shoot-through modes. The shoot-through zero state is provided by the LC and diode network. This network defends the circuit from damage during the shoot-though zero state by storing energy in L and C. The qZS network boosts the dc-link voltage with the help of stored energy in the network elements.

The power is transmitted from dc side to ac side during non-shoot-through mode. There is no power transmission during shoot-through state since the dc-link voltage is zero. The equivalent circuit of the non-shoot-through and shoot-through operating modes are disclosed in the Fig.3a and Fig.3b, and the polarities are made known with arrows. One switching cycle is represented by T, and is given by $T = T_0 + T_1$, where T_0 is the interval of the shoot-through mode and T_1 is the interval of non-shoot-through mode. The shoot-through duty ratio is given by $D = T_0 / T$

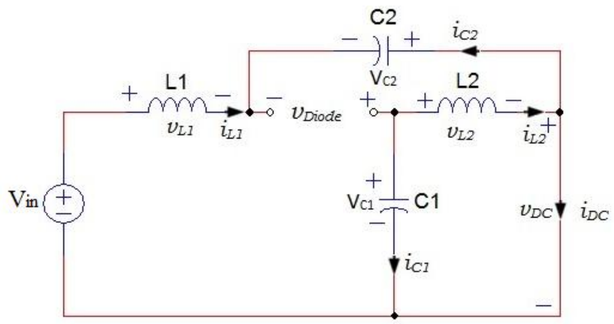

Fig.3a. Equivalent circuit of qZS-MCMLI in shoot-through state

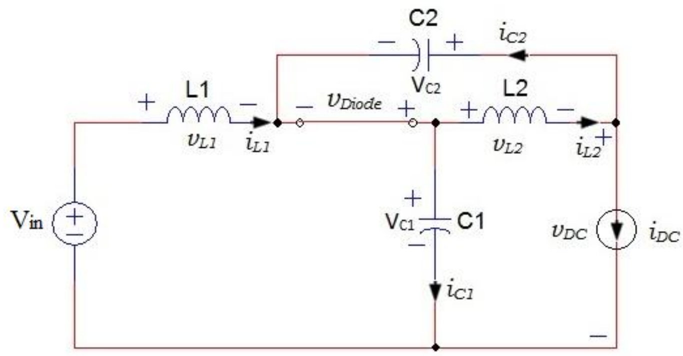

Fig.3b. Equivalent circuit of qZS-MCMLI in non shoot-through state

The fundamental equations governing the operation of the qZS-MCMLI are given below. The average value of the voltage across capacitor C_1 is given in (1)

$$V_{C1} = \frac{1-D}{1-2D} V_{in} \tag{1}$$

The average value of the voltage across capacitor C_2 is given in (2)

$$V_{C2} = \frac{D}{1-2D} V_{in} \tag{2}$$

The average value of the currents through the inductors L_1 and L_2 are given in (3)

$$I_{L1} = I_{L2} = \frac{1-D}{1-2D} V_{in} \tag{3}$$

The average value of DC link voltage is given in (4)

$$v_{DC} = \frac{1}{1-2D} V_{in} = B V_{in} \tag{4}$$

The average value of AC output voltage is given in (5)

$$v_{ac} = M \cdot B \cdot \frac{V_{in}}{2} \tag{5}$$

The boost factor B is given in (6)

$$B = \frac{1}{1-2D} \tag{6}$$

The voltage gain G is given in (7)

$$G = M \cdot B \tag{7}$$

Where, M is the modulation index and V_{in} is the input dc voltage to the qZS network.

Each boosted voltage from the qZS network is connected in cascade with other boosted voltages through the half bridge cell comprising of one active switch and one diode that can generate multilevel positive output voltage. The full H-bridge unit is connected with the cascaded auxiliary units to acquire both positive and negative multilevel positive output voltage. The output voltage +1Vdc (first level) is produced across the load when switching on controlled switches Sa2, Sb2, Sc1, S1 and S2, and maintaining the remaining switches in off state. The output voltage +2Vdc (second level) is produced across the load by turning on the switches Sa2, Sb1, Sc1, and S2. Similarly, the output voltage +3Vdc is obtained by switching on Sa1, Sb1, Sc1, S1 and S2. In a nutshell, it is observed that the input DC voltage from renewable energy sources can be boosted by the qZS network and converted into a stepped DC voltage by the half bridge cell, which is further processed by the full H Bridge unit to generate approximately sinusoidal AC waveform.

III. Multicarrier Pulse Width Modulation Techniques For QZS-MCMLI

There are various MCPWM methods available for controlling the qZS-MCMLI. These can be classified into two major categories such as Phase Shifted (PS-PWM) and Level Shifted (LS-PWM). For an n level multilevel inverter utilizing the LS-PWM, n -1 carrier is needed, where these multiple carriers are arranged in vertical shifts to cover the entire amplitude range of the reference signal. The reference signal can be a sinusoidal signal. Multiple triangular carrier waves are compared with the single Sinusoidal reference wave in these Multi carrier PWM schemes. In phase disposition pulse width modulation (PD-PWM), the carriers are in phase with each other. In phase opposition disposition (POD-PWM), the positive carriers are arranged in phase with each other and the negative carriers are arranged in opposite phase. The alternate phase opposition disposition (APOD-PWM) is formed by alternating the phase between adjacent carriers [8]. If C is the number of carrier waveforms, then the number of carriers required to produce N level output is (C-1). The sinusoidal reference signal has amplitude of Am and a frequency fm. The multiple triangular carrier waves are having same peak to peak amplitude Ac and frequency fc. The single sinusoidal reference signal is continuously compared with all the carrier waveforms. A pulse is generated if the sinusoidal reference signal is greater than the carrier signal during comparison. The frequency ratio mf is given by Mf = fc/fm. In this paper, the MCPWM methods such as PD-PWM, POD-PWM are APOD-PWM are analysed in conjunction with the proposed qZS-MCMLI and simple boost control though there are so many carrier wave arrangements are available in the literature. The shoot-through states are generated by the simple boost control technique, where two constant lines with magnitude equal to or greater than the peak value of the sinusoidal reference signal are used to control the shoot-through duty cycle. The shoot-through states are developed when the high frequency triangular carrier is greater than the upper straight line or lesser than the lower straight line. By varying the amplitudes of these constant lines, shoot-through duty ratio and boost factor can be varied. In PD-PWM, all carriers have same frequency fc and same amplitude Ac. The carriers are arranged such that the areas they cover are contiguous. In this technique, extensive harmonic energy is focused at a carrier frequency without emerging to the output voltage. The reference signal with an amplitude Am and frequency fm is compared with each of the carrier signals to generate gate pulses. The sinusoidal reference signal, the triangular carrier signals, and constant lines for simple boost controller are shown in Fig. 4.

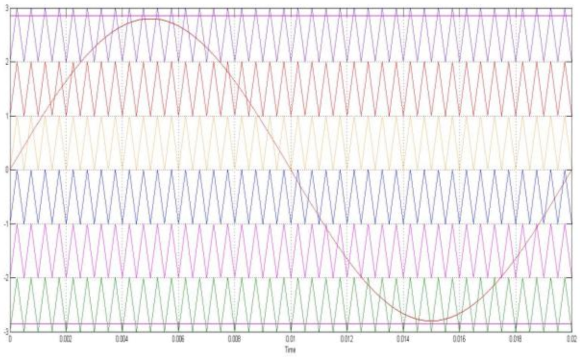

Fig.4. Phase Disposition PWM Scheme (PD-PWM)

IV. Simulation Results

In this paper, simulations have been performed using MATLAB/SIMULINK to analyze the capabilities of the proposed multilevel inverter and their simulation results were presented. The design parameters for the proposed new topology are provided in table I. The simulation model of the proposed topology is shown in Fig.5. The output voltage and FFT spectrum of the new qZS-MCMLI with reduced number of switches are presented in the Fig.6 and Fig.7.

Table I. Simulation parameters of the qZS-CHB-MLI

Input dc voltage	V_{in}	100V
qZS network	$L=L_1=L_2$	40 mH
	$C=C_1=C_2$	2000 µF
Switching frequency	f_S	10 KHz
Resistive Load	R_L	50Ω

For the DC input voltage V_{in} of 100V for each quasi-Z-Source network and the shoot-through duty ratio D of 10% and the fundamental RMS output voltage of 246.2V is obtained and it is presented in Fig.6. The voltage across the capacitors C1 and C2 are shown in Fig.8. and DC link voltages of the proposed topology are given in Fig.9.

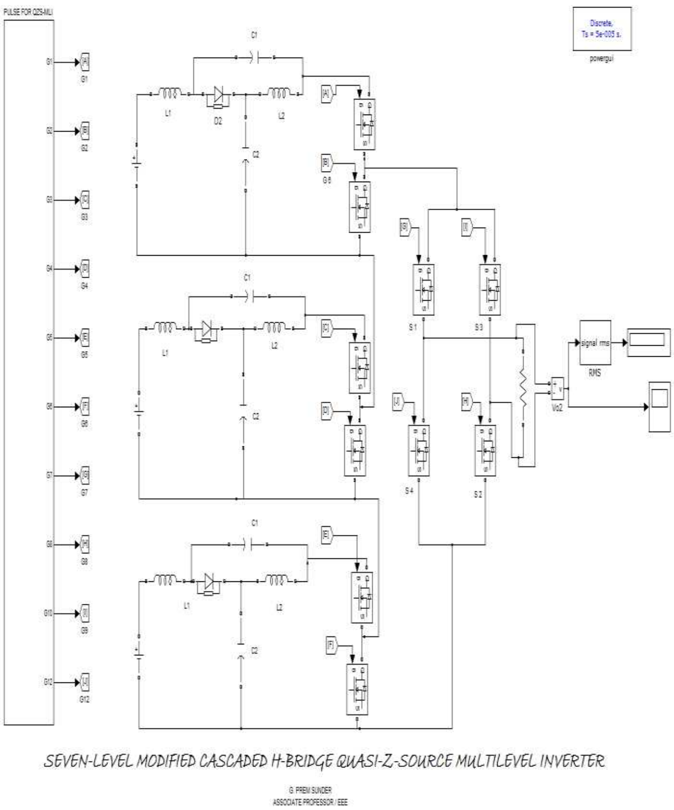

Fig.5 Simulation Module of qZS-MCMLI

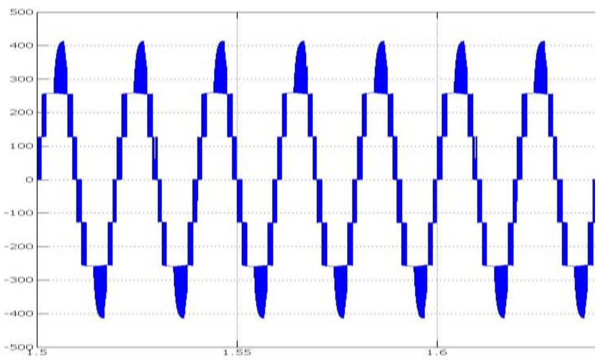

Fig.6 Output voltage of qZS-MCMLI

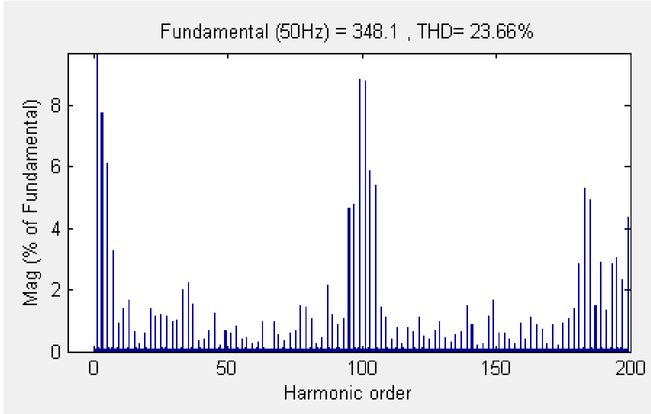

Fig.7 FFT spectrum of Output voltage waveform

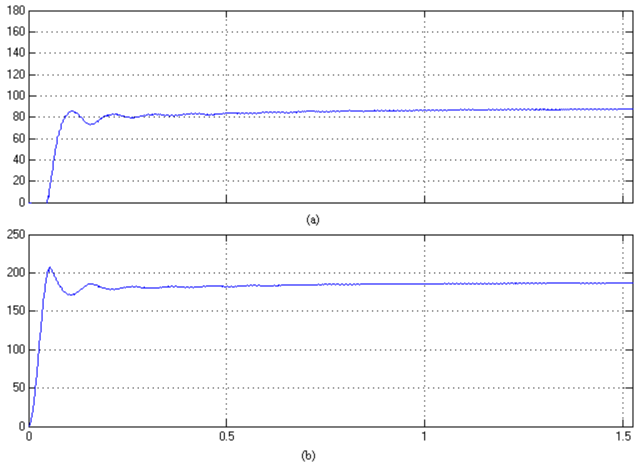

Fig.8 Voltage across the (a) capacitor $C_1$and (b) Capacitor C_2

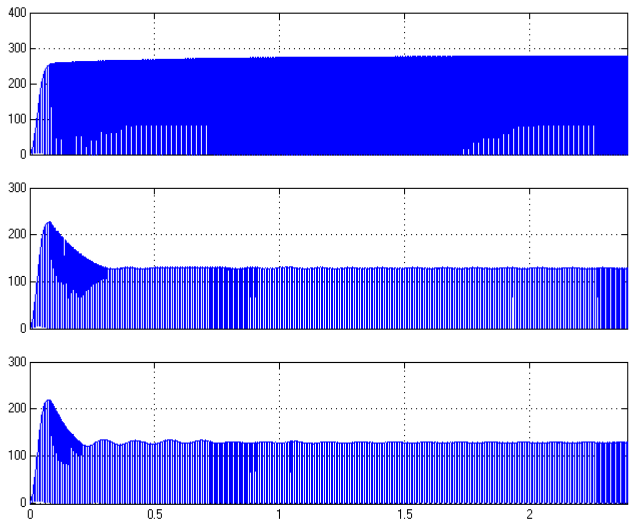

Fig.9 DC link voltage of the proposed topology

V. Conclusion

The proposed qZS-MCMLI topology provides attractive advantages like reduced number of switches, voltage boost ability not limited to input voltage (DC source) summation, reduced THD, single stage conversion and reliability against short-circuits. Using PD-PWM control method, the qZS-MCMLI performance parameters are analysed and presented. The PD-PWM control method combined with simple boost control technique provides better THD. This proposed qZS-MCMLI topology is more suitable and can be effectively used for PV based applications.

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