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Forward Error Control System Performance of Maximum Free Distance Convolutional Codes with Different Modulation Schemes

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***Abstract*— Forward Error Control (FEC) based on Convolution Encoders with Viterbi decoding is a good methodology to decrease the effect of Additive Gaussian Noise residing inside digital data transmissions channel. In this paper a Convolutional encoders with maximum free distance and different constraint lengths have been tested with AWGN channel effect using MATLAB. The performance and analysis has done by changing rates of Convolutional encoders and different constraint lengths and take in consider QPSK, 16-QAM and 64-QAM as modulation schemes.**

***Index Terms*— Additive White Gaussian Noise (AWGN), Convolutional Encoder, Trellis Diagram, QPSK, 16-QAM and 64-QAM Modulation.**

I. Introduction

Convolutional codes are introduced in 1955 by Elias. Convolutional codes are one of the powerful and widely used class of codes, These codes are having many applications, that are used in deep-space communications, voice band modems, wireless standards(such as 802.11) and in satellite communications. Convolutional codes are plays a role in low-latency applications such as speech transmission [1].

II. Convolutional Encoders

A. Convolutional Encoders Structure

Convolutional encoder of (n, k) is defined by $k \times n$ matrix, where k is input bits and n output bit so Convolutional encoder information rate of k/n. An important parameter of Convolutional encoder is their constraint length which is corresponds to the total size of their internal memory [2]. This parameter is important in Viterbi decoding algorithms complexity since it means more states in convolutional encoder trellis. In Convolutional encoder the message stream input to encoder continuously and run through it. Thus the Convolutional encoder required very little buffering and storage hardware [3]. Convolutional encoder parameters notation used in this paper as following

n = number of output bits.
k = number of input bits.
m = number of stages of shift registers.
L = number of bits in message sequence.
u = input bits.
Constraint Length: K = (m + 1) digits.
Code Rate: r = k/n.
Shift register = D.

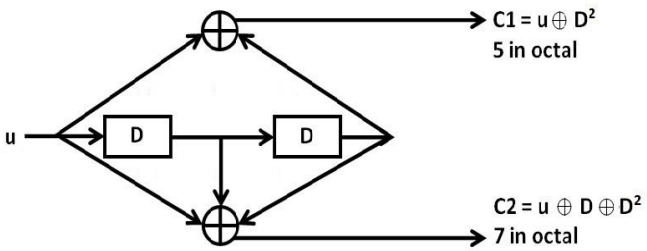

Fig.1. Convolutional encoder of code rate ½, constraint length K = 3, Generator polynomials of {5, 7} octal.

The generator polynomials of Convolutional encoder represent the connections between shift registers. To generate the output code a mode two addition (EX-OR) between shift registers contents are performed. The output code is the results of generator polynomials C1C2. In Convolutional encoders common transition table calculations take in consider the input bit and shift register contents in present state and next state illustrate the generation of output code. For Fig.1, Convolutional encoder Table 2, show transition calculations.

Table 1. Transition table calculations of output code C1 and C2, rate ½, K=3, generator {5, 7} octal.

Input	Present state			Next state			Output	
U	D1	D2	State	D1	D2	State	C1	C2
0	0	0	a	0	0	a	0	0
1	0	0	a	1	0	c	1	1
0	0	1	b	0	0	a	1	1
1	0	1	b	1	0	c	0	0
0	1	0	c	0	1	b	0	1
1	1	0	c	1	1	d	1	0
0	1	1	d	0	1	b	1	0
1	1	1	d	1	1	d	0	1

The notation of states as a, b, c and d. is to simplify the point of view for Convolutional encoder trellis states.

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B. Convolutional Encoder state diagram

In refer to Table 1. Convolutional encoder state diagram could be constructed by joining the input bit with the output resulted code starts from present state to next state. See Fig. 2.

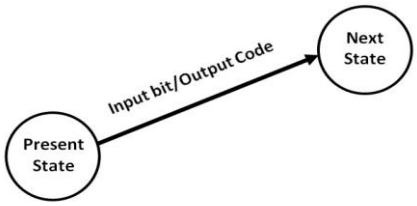

Fig.2 State transition illustration

According this demonstrated simple rule shown in Fig.2. Then full description of Convolutional code trellis diagram of Figure 1 is presented in Fig.3 below.

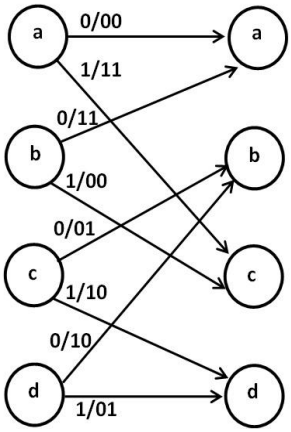

Fig.3 Convolutional code trellis diagram, code rate ½, constraint length K=3, generators {5, 7}.

In case increasing constraint length. The number of shift registers increased too. The convolutional encoder calculations remain in same steps. Take for example convolutional encoder with the same code rate of ½, but with constraint length increased to K=4. Then the number of shift registers rose to 3, Generator polynomials {15, 17} see reference [4] for convolutional encoders table.

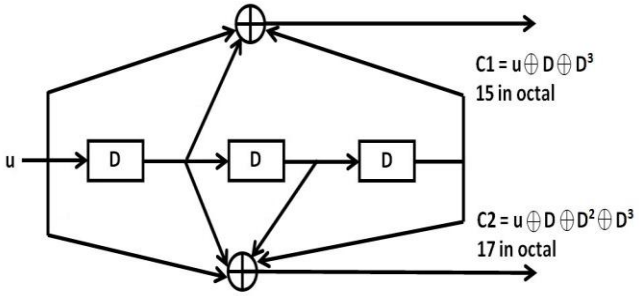

Fig.4 Convolutional encoder of code rate ½, constraint length K = 4, Generator polynomials of {15, 17} octal.

The transition table gives eight states, as shown in Table 2. This increasing in number of states reflected on Viterbi decoding complexity.

Table 2. Convolutional encoder transition table illustrate calculations of output code C1 and C2, code rate ½, K=4, generator {15, 17} octal.

Input	Present state				Next state				Output	
U	D1	D2	D2	State	D1	D2	D3	State	C1	C2
0	0	0	0	a	0	0	0	a	0	0
1	0	0	0	a	1	0	0	e	1	1
0	0	0	1	b	0	0	0	a	1	1
1	0	0	1	b	1	0	0	e	0	0
0	0	1	0	c	0	0	1	b	1	0
1	0	1	0	c	1	0	1	f	0	1
0	0	1	1	d	0	0	1	b	0	1
1	0	1	1	d	1	0	1	f	1	0
0	1	0	0	e	0	1	0	c	1	1
1	1	0	0	e	1	1	0	g	0	0
0	1	0	1	f	0	1	0	c	0	0
1	1	0	1	f	1	1	0	g	1	1
0	1	1	0	g	0	1	1	d	0	1
1	1	1	0	g	1	1	1	h	1	0
0	1	1	1	h	0	1	1	d	1	0
1	1	1	1	h	1	1	1	h	0	1

And convolutional encoder trellis had shown in Fig. 5.

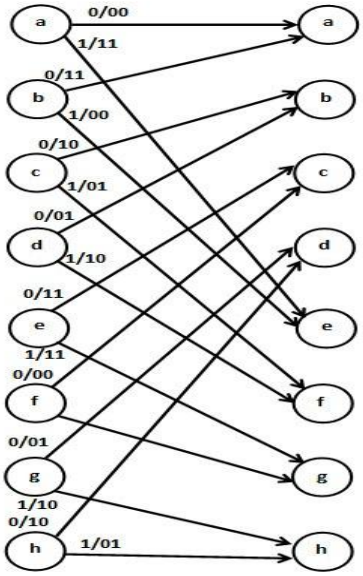

Fig.5 Convolutional code trellis diagram, code rate ½, constraint length K=4, generators {15, 17}.

The convolutional encoder parameter denoted by d_{free} [5], refers to convolutional encoder free distance that can be interpreted as the minimal length of an erroneous "burst" at the output of a convolutional decoder [6]. The fact that errors appear as "bursts" should be accounted for when designing a concatenated code [7]. If assumed for another application an inner convolutional code. The common solution for this problem is to interleave data before convolutional encoding [8], so that the outer block (such as Reed-Solomon) code can correct most of the errors. The interleaver also shown in Turbo code application placed between two convolutional encoders. In hardware implementation of convolutional encoder, FPGA used to implement both convolutional encoder and Viterbi decoder see references [9] and [10]. Convolutional encoders applied in many digital transmission applications, the tested convolutional encoders in this paper represent also so called mother codes.

From which the puncturing process applied to convolutional encoders to produce different data rates that

matched to the needed digital transmission data rates [11].

III. Forward Error Control System

The system considered in this paper consist of outer convolutional encoder and modulation scheme of QPSK, the transmission channel is Additive White Gaussian Noise (AWGN), the receiver side use demodulation process then Viterbi decoder [5]. See Fig. 6.

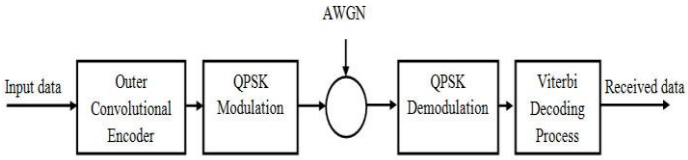

Fig. 6, show Forward Error Control System (FEC).

IV. Simulation Results and Discussion

The simulation test performed with different convolutional encoder's rates and constraint lengths, the figures below show the simulation results. The simulation program flow chart is shown in Fig. 7:-

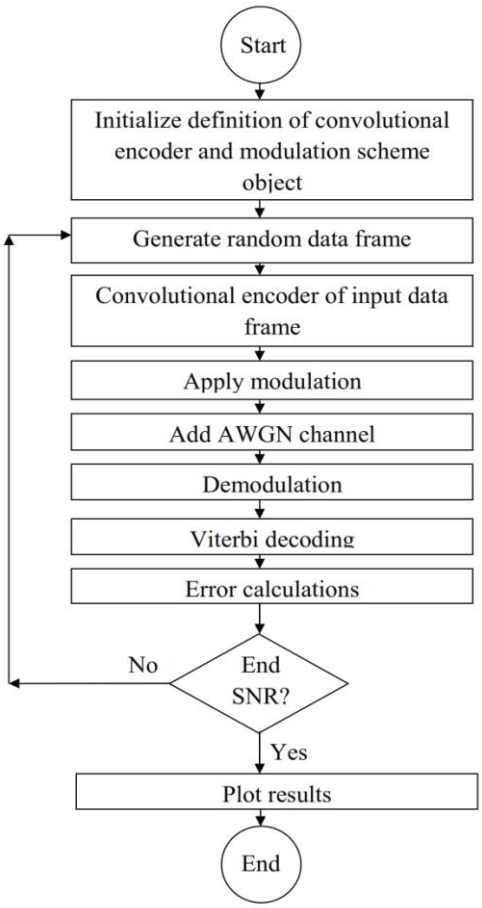

Fig. 7. Simulation program flow chart.

Simulation results listed in figures from 8 to 19.

IV. Conclusion

From simulation results, the increasing constraint length with increasing free distance of convolutional encoder show improvement in bit error rates BER performance. But this improvement in performance come with important consideration related to Viterbi decoder complexity growth. So the choice of convolutional encoder may take two consideration first the application data rates and the second the important of the application and its cost. The modulation schemes used such as QPSK applied in low data rates where 16-QAM and 64-QAM are useful with higher data rates hence 16-QAM consist of 4 bits per symbol and 64-QAM 6 bits per symbol. The investigated modulation types represent standard modulation types used with modern application such as 'LTE' long term evolution.

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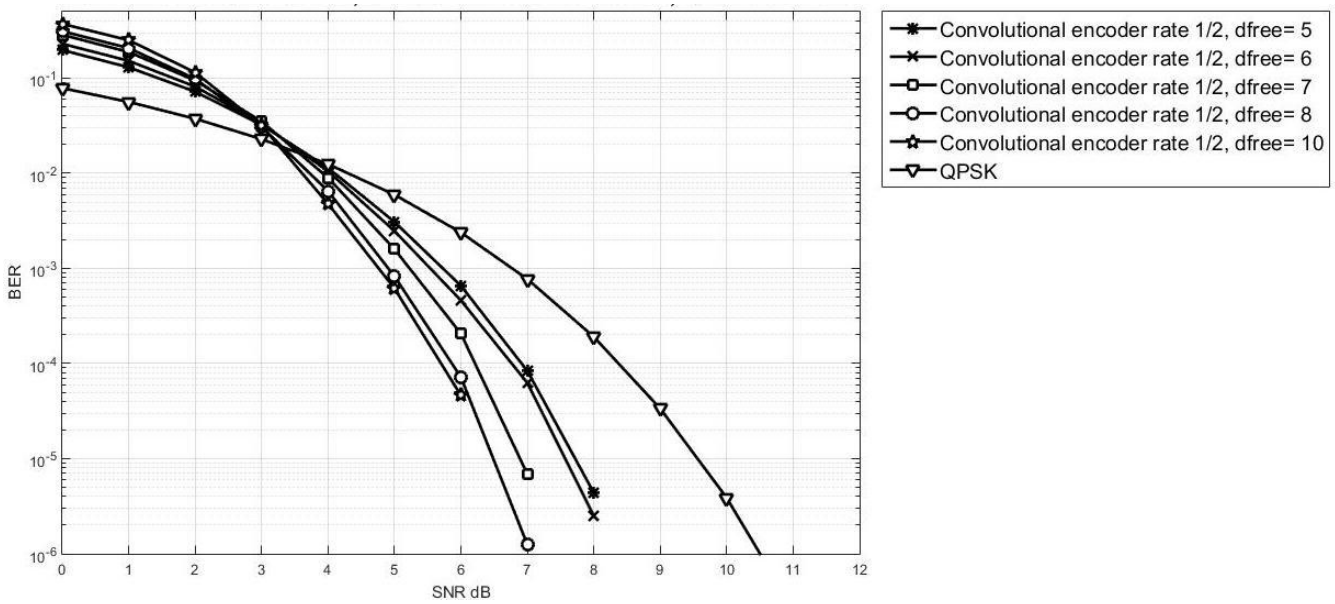

Fig. 8. FEC system tested with rate ½ convolutional encoders and QPSK.

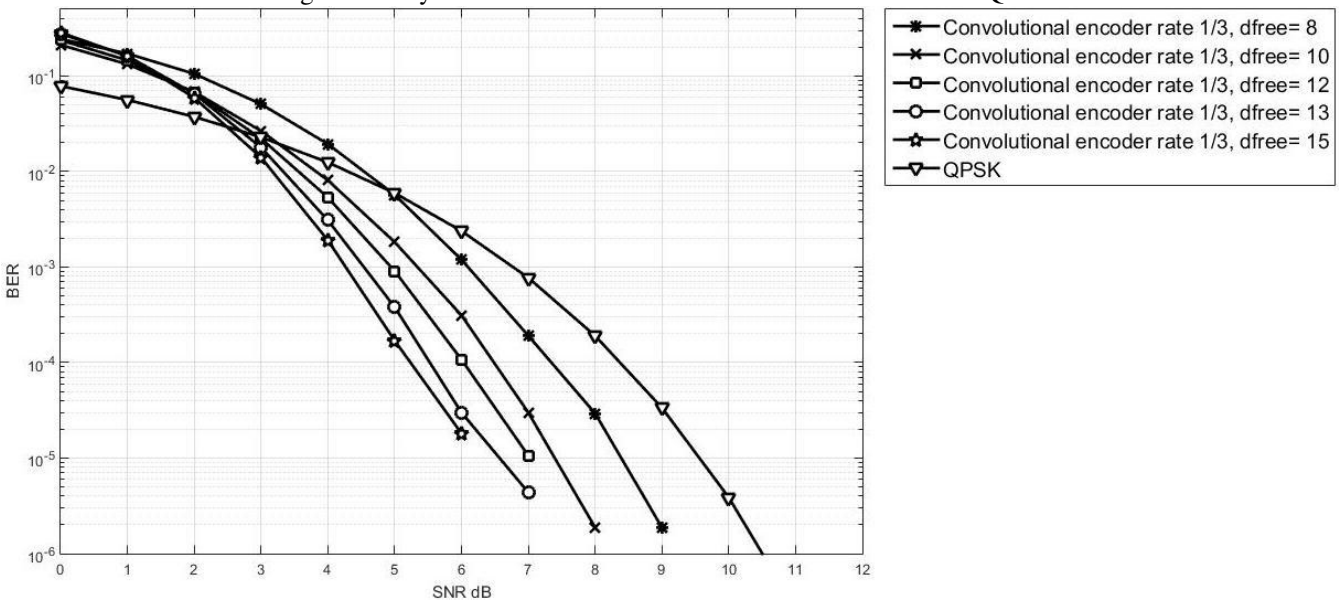

Fig. 9. FEC system tested with rate 1/3 convolutional encoders and QPSK.

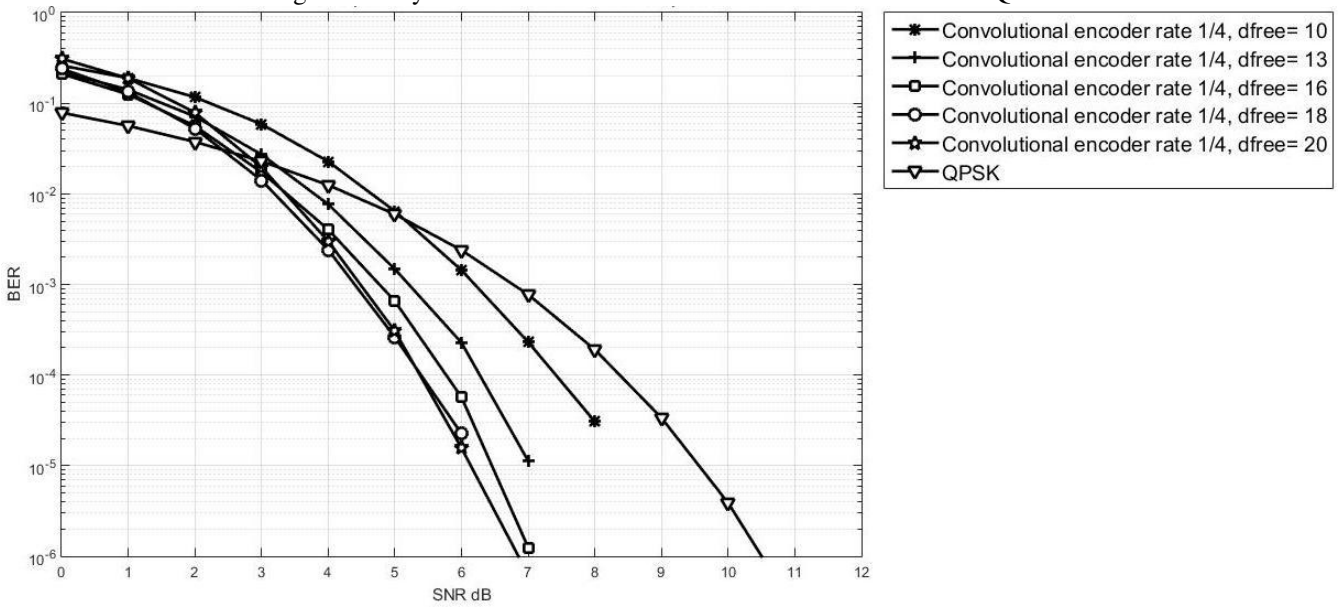

Fig. 10. FEC system tested with rate 1/4 convolutional encoders and QPSK.

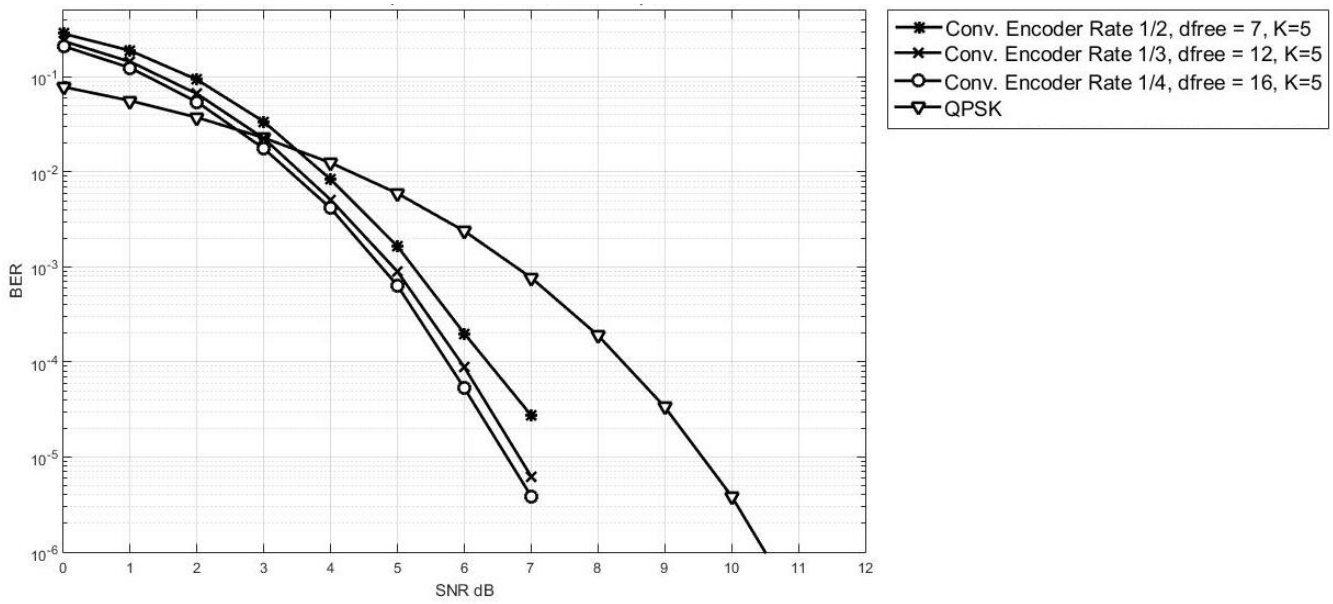

Fig. 11. FEC system comparison between different code rates with QPSK

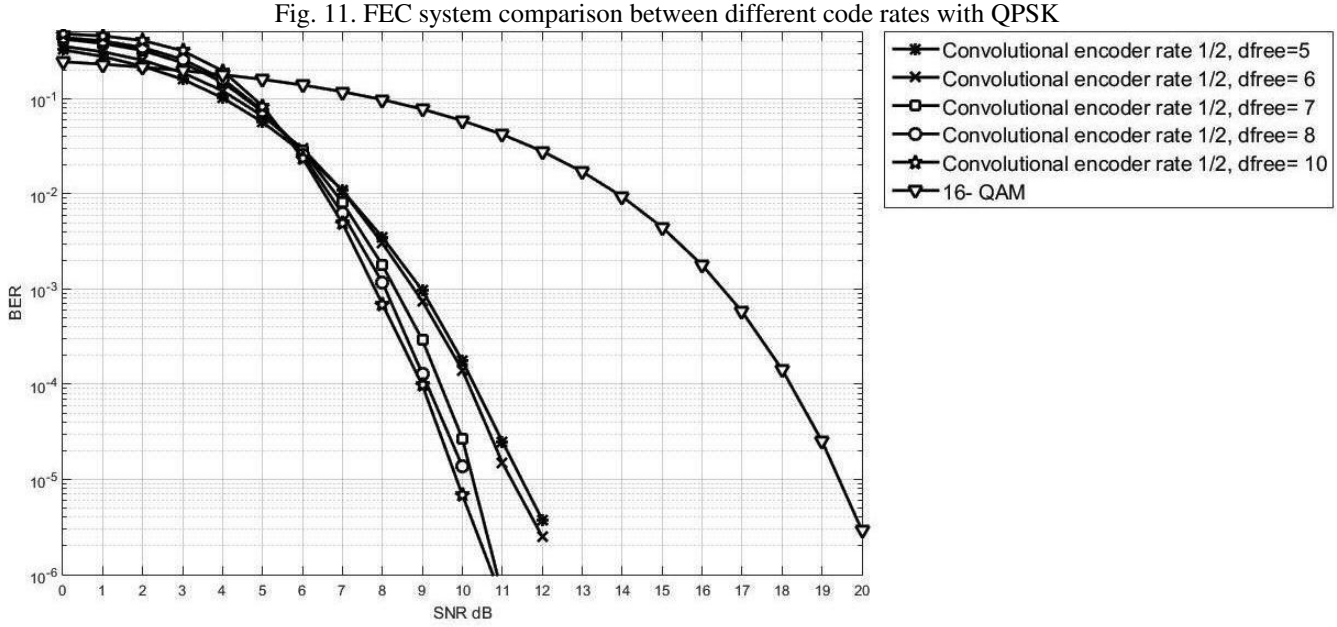

Fig. 12. FEC system tested with rate 1/2 convolutional encoders and 16-QAM.

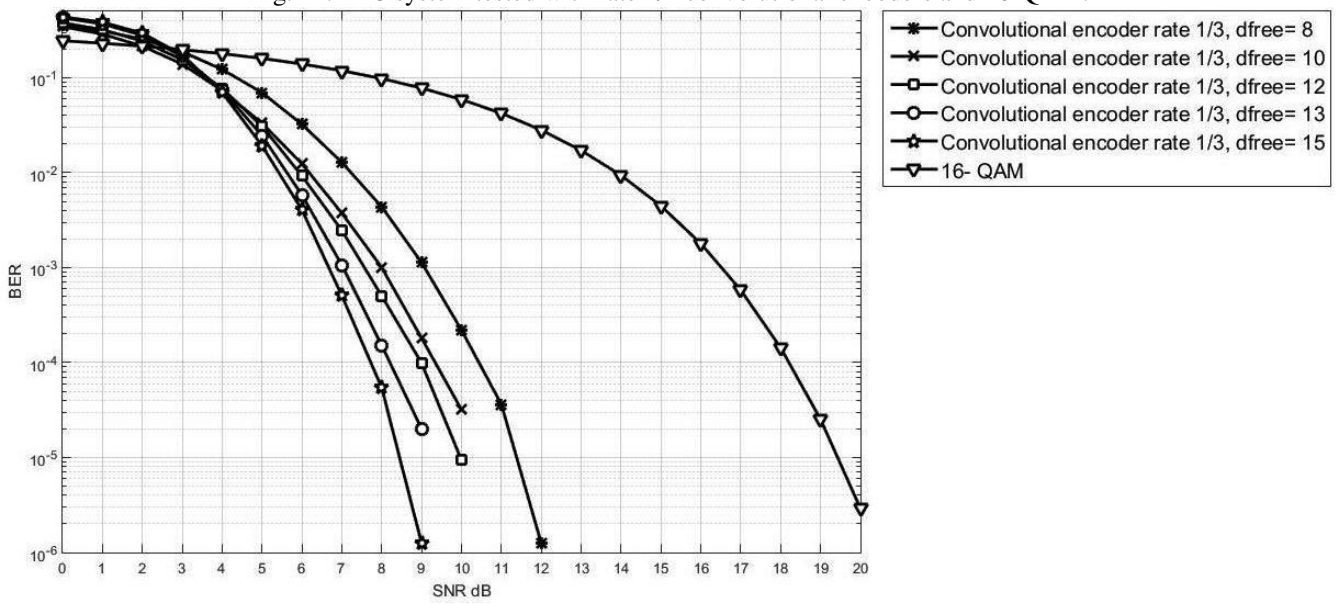

Fig. 13. FEC system tested with rate 1/3 convolutional encoders and 16-QAM.

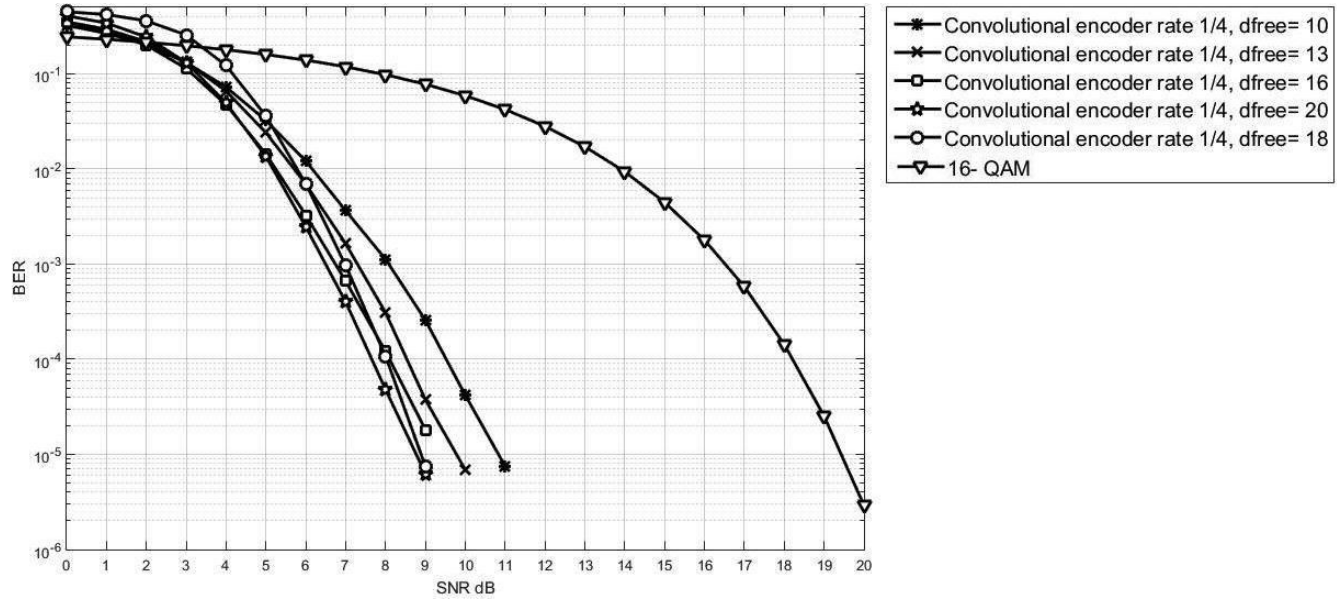

Fig. 14 FEC system tested with rate 1/4 convolutional encoders and 16-QAM.

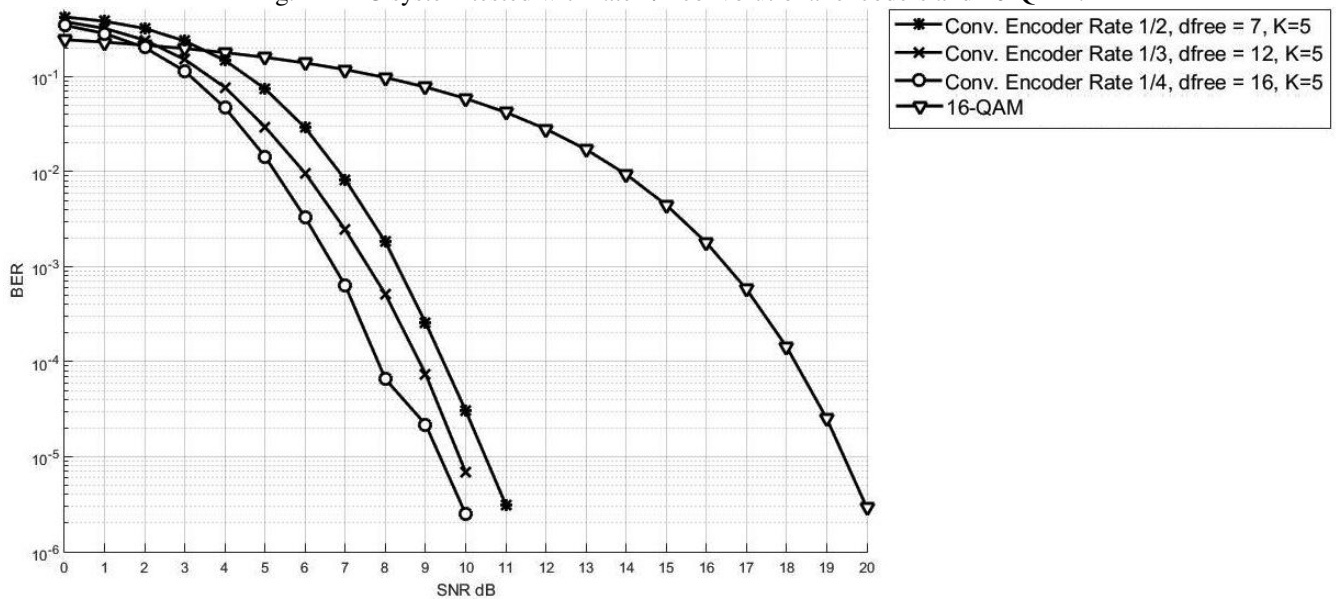

Fig. 15. FEC system comparison between different code rates with 16-QAM

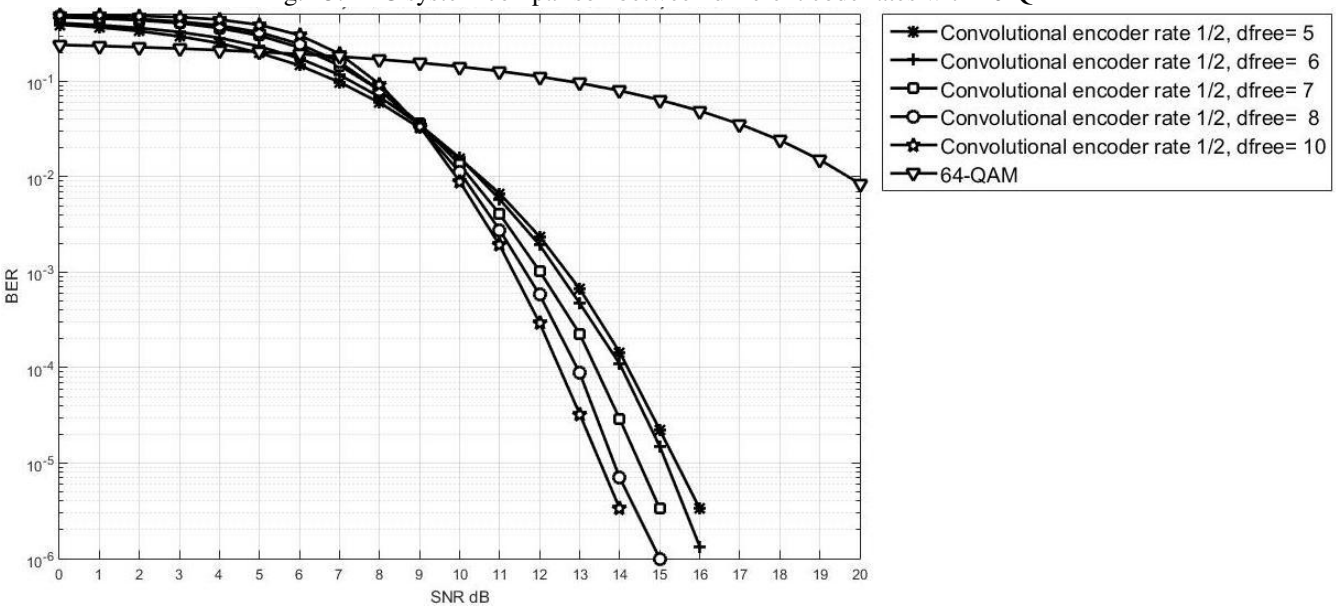

Fig. 16. FEC system tested with rate 1/2 convolutional encoders and 64-QAM.

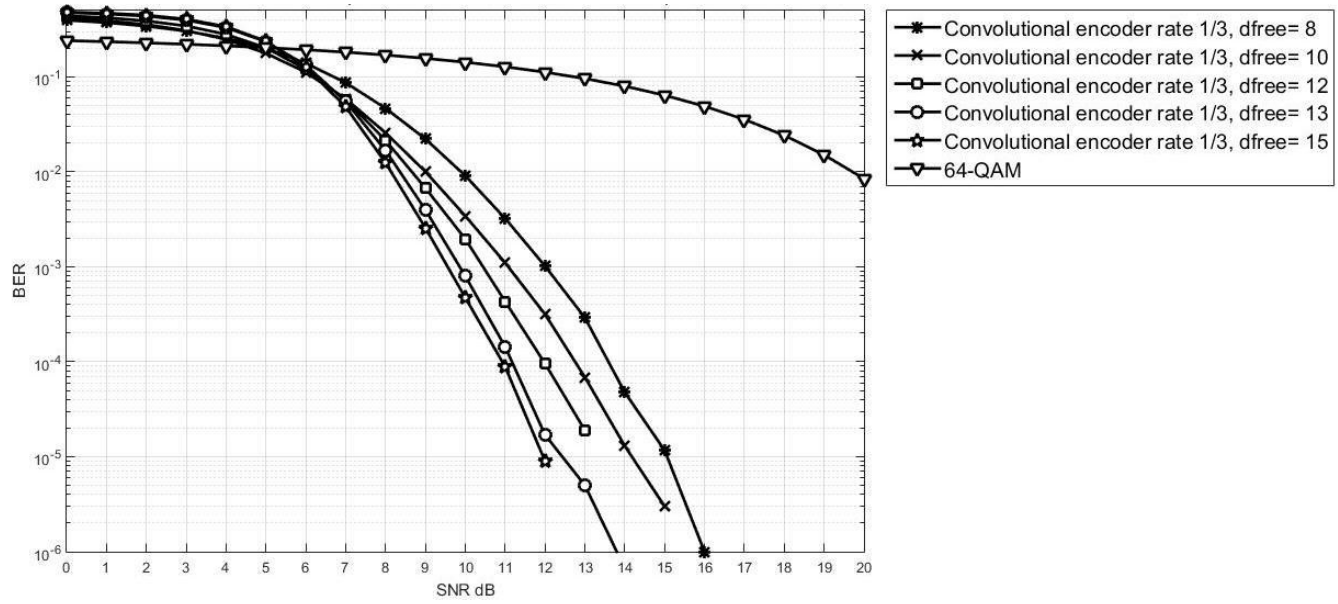

Fig. 17. FEC system tested with rate 1/3 convolutional encoders and 64-QAM.

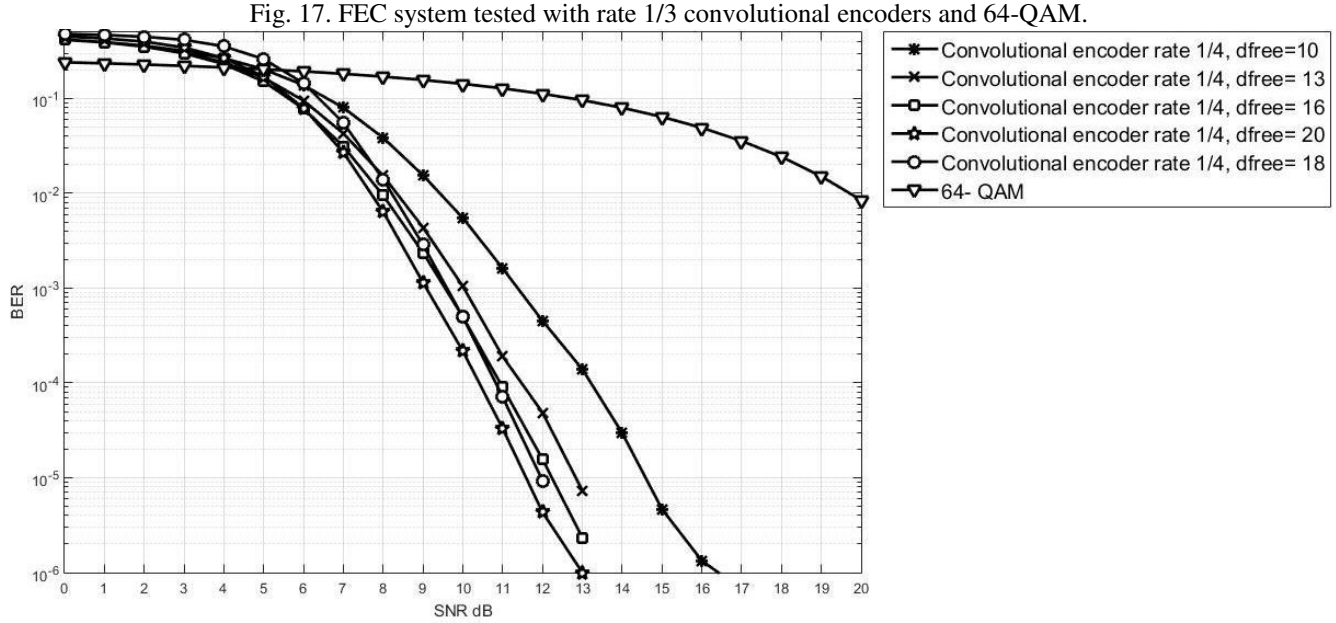

Fig. 18. FEC system tested with rate 1/4 convolutional encoders and 64-QAM.

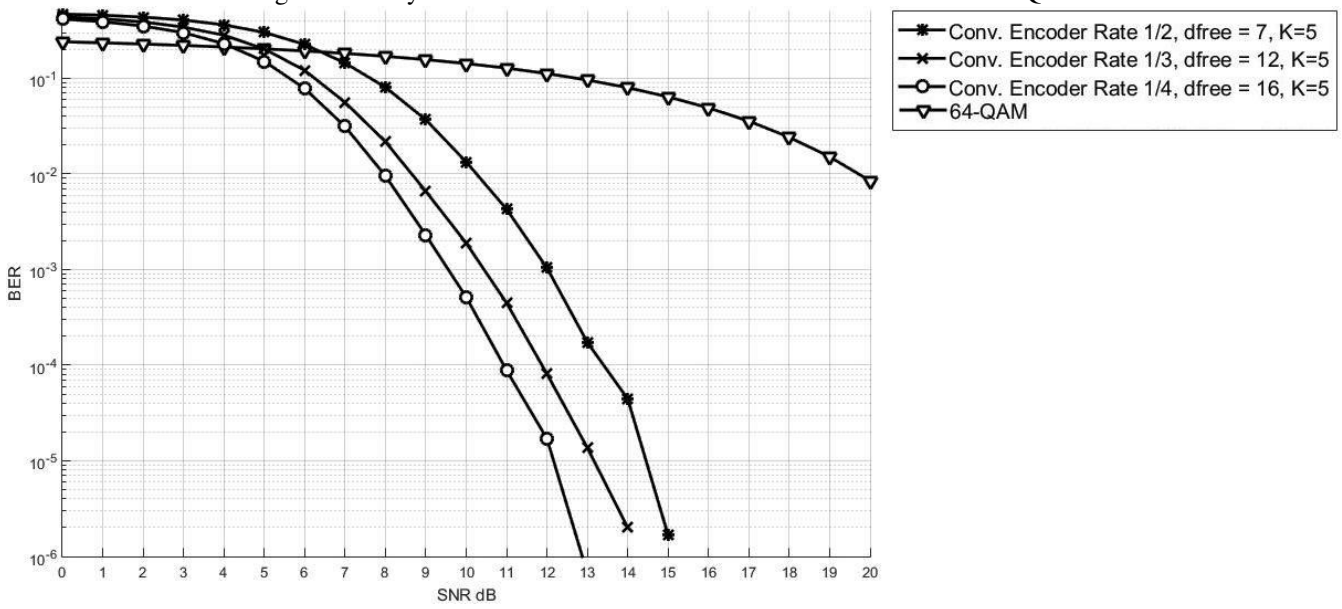

Fig. 19. FEC system comparison between different code rates with 64-QAM