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A Simple Method to Obtain the Generation Lifetime in MOS Capacitors

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Abstract—**This paper describes a new simple method for the estimation of the generation lifetime in MOS capacitors fabricated on high resistivity silicon substrates. In this method, the transition between the strong inversion initial steady state and the non-equilibrium deep depletion state occurs by applying a triangular gate voltage. The mathematical model of the proposed method is presented. The generation lifetime value, τ_g = 517 ± 40 µs, obtained with our current-triangular sweep voltage method agrees with the 510 ± 30 µs value obtained by the *C-t* Zerbst method, and the 517 ± 15 µs value obtained by using the *I-C-t* characteristics for a pulsed MOS capacitor. The results obtained in this work show that the proposed simple method is useful as an express monitoring tool for an estimation of the generation lifetime.**

Index Terms **Current-Triangular Sweep Voltage Method, non-equilibrium deep depletion, generation lifetime, MOS capacitor.**

I. Introduction

The pulsed metal-oxide-semiconductor (MOS) capacitor transient [1] is the most frequently method used to determine the minority carrier generation lifetime and the surface generation velocity. Several methods for investigate the generation lifetime in MOS capacitor have been developed: current-capacitance (*I-C-t*) [1], Zerbst capacitance-time (*C-t*) technique [3], and linear sweep techniques [4], among others [6]. The knowledge of the generation lifetime τ_g is important for monitoring technological processes for device fabrication based on high-resistivity silicon substrates as photodetectors, particles counters, and charge coupled devices (CCD). This is due to the strong dependence of the device performance on the substrate characteristics such as the crystalline defects density, heavy metal atoms contamination, and the interface state density [1], parameters that can be strongly changed during the chemical and high temperature technological processes.

Unfortunately, those methods mentioned above require the use of specialized and expensive measuring equipment. In the Zerbst technique, the MOS capacitor is pulsed into the deep depletion state. The time-dependent relaxation of the depletion layer width is related to the change in the inversion layer carrier density, and from the capacitance relaxation by thermal electron-hole generation; in this way the minority carrier generation lifetime can be determined. The substrate doping density needs to be known. However, when simultaneous *C-t* and *I-t* curves are measured, the generation time can be determined without knowing the doping concentration. The equilibrium between the thermal electron-hole generation rate and the linearly varying voltage driving the device into deep depletion is used in the linear sweep technique [4]. A series of $C\text{-}V_G$ curves at different linear sweep rates, *R*, are necessary to determine the generation lifetime.

In this work, a simpler method for the estimation of the generation lifetime, that requires only a function signal generator and a digital oscilloscope, is proposed. The mathematical modeling of the non-equilibrium processes occurring in the MOS capacitor using such method is described. To validate the model, the generation time obtained with this method is compared with the results obtained with other well-known methods.

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II. Operating Principle

A. Model considerations

In order to obtain the generation lifetime of minority carries in MOS capacitors by *our current-triangular sweep voltage method*, the capacitor is connected in series with a function generator having a DC offset voltage and a load resistor R_L. The superposition of the constant (DC) voltage $U_1 < 0$ and the triangular voltage signal, with period $2T$, is applied to the gate of the MOS capacitor, which was fabricated on an n-type silicon substrate.

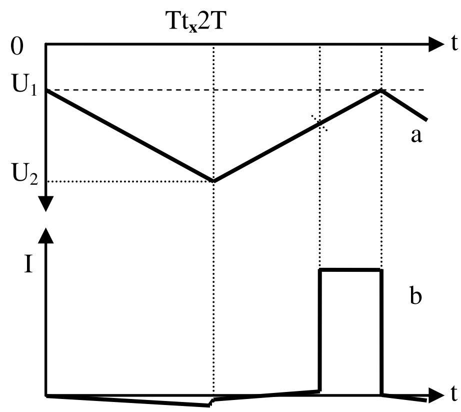

Fig. 1. Time-dependent gate voltage (a) and the current (b) flowing through the circuit.

The output signal is recorded by a digital oscilloscope. Under accumulation, the MOS capacitor presents a capacitance of C_{ox}. The constant negative voltage U_1 applied to the gate leads the capacitor to a strong inversion initial steady state. The triangular voltage $U_2(t)$ with the same sign as U_1 leads the capacitor to a non-equilibrium deep depletion state. The time-dependent gate voltage (a) and the current (b) flowing through the circuit are shown schematically in Fig. 1.

If both surface contributions to the generation are minimized (the peripheral surface and the surface states at the Si/SiO_2 interface), three current components will flow through the circuit: a displacement current $I_d = C(t)\, dU/dt$ produced by the variation of the capacitance due to the variation of the depletion region width, a current I_g due to the generation of carriers from the deep levels inside the depletion region, and a current I_{diff} due to the diffusion of carriers coming from the neutral volume of the substrate. The sign of the total current is different for the two half periods: at the first half period the total current is $-I_d-I_g-I_{diff}$ due to the coincidence of their individual signs; on the other hand, at the second half period, the total current changes its sign at a certain time because here I_d is always positive whereas (I_g + I_{diff}) is negative.

At the first half-period, the increase of the total negative voltage from U_1 to U_2 leads to a time-dependent increase of the depletion region width, from its steady value W_{inv} (determined by the offset U_1) to its maximum at $t = T$. The thermally generated minority carriers as well as the minority carriers diffusing from the neutral volume fill the potential well created by the increasing negative total voltage, from U_1 to U_2, which leads to a decreasing width for the depletion region. If the current components I_g and I_{diff} due to the flow of these carriers are not too high, the potential well will not be filled completely, and this process may continue at the beginning of the second half-period. The point where the total current crosses the axis means that $I_d = -(I_g + I_{diff})$. After this time, I_d continues being positive and higher than the other two negative contributions; and at the time $t = t_x$, and due to the decreasing width of the depletion region to its initial value W_{inv}, the displacement current becomes constant to a value $I_d = C_{ox} dU/dt$.

B. Mathematical modeling

In *the current-triangular sweep voltage method*, the mathematical modeling of these non-equilibrium processes is useful to determine the carrier generation time in MOS capacitors fabricated on high resistivity substrates. For the time interval $0 < t < T$, the applied triangular voltage can be described as

$$U(t) = U_1 + \Delta U \frac{t}{T}, \quad \Delta U = U_2 - U_1 \tag{1}$$

and for the time interval $T < t < 2T$ as

$$U(t) = U_1 + \Delta U \left(\frac{2T - t}{T} \right) \tag{2}$$

The absolute value of the triangular sweep voltage is considered in the mathematical modeling. When the additional voltage $U(t)$ is applied, the steady initial inversion state of the MOS capacitor is broken due to the formation of a new non-equilibrium deep depletion state with a depletion width $W(t) = W_{inv} + w(t)$. Thus, at the first half period, the depletion width began to increase from the value W_{inv} to the value $w(T)$. The formation of a deep potential well in the absence of illumination is accompanied with the filling of this well by carriers thermo-generated in the additional depletion layer $w(t)$ and diffused from the neutral volume of the substrate. Generally, under these conditions the time variation of the inversion layer charge, Q_p, is

$$\frac{dQ_p}{dt} = I_g + I_{diff} = \frac{q n_i w(t) A}{\tau_g} + I_{diff} \tag{3}$$

where q is the electron charge, n_i is the intrinsic carrier concentration in the substrate, A is the area of the MOS capacitor, and τ_g is the generation lifetime. In this work, we assume that at room temperature the diffusion component in Equation (3) is much lower than the generation component, which usually is quite high for silicon [1].

If the generation rate through the deep levels within the depletion region $w(t)$ and the diffusion of minority carriers from the neutral volume of the substrate are very high, the potential well is filled during the first half-period of the applied voltage $U(t)$. At low generation values, the filling of the potential well will occur during some time interval at the second half-period even though the depletion width has decreased.

From the second Kirchhoff's law for the circuit containing the MOS capacitor connected in series with the function generator and a load resistor R_L, the basic equations are:

$$U(t) = \frac{Q_p}{C_{ox}} + U_p + U_n + \frac{q N_d w^2(t)}{2\varepsilon_0 \varepsilon_s} \tag{4}$$

Here, Q_p is the charge of the inversion layer at the voltage U_1; U_p and U_n are the voltage drops in the inversion and depletion layers at the voltage U_1, respectively, $C_{ox} = \varepsilon_0 \varepsilon_{ox} A / d_{ox}$; ε_0, ε_{ox}, ε_s are the permittivity of vacuum, oxide, and substrate, respectively, d_{ox} is the oxide thickness, A is the gate area, and N_d is the donor concentration in the substrate. The voltage drops U_p, U_n and the load resistor for $R_L < 50$ kΩ are very low for a current level below 10^{-5} A when compared to $U(t) - U_1 > 5$V (using absolute values). By solving (3) and (4), we obtain the equation $w(t) \cong w$:

$$w \frac{dw}{dt} = \frac{\varepsilon_0 \varepsilon_s}{q N_d} \frac{dU}{dt} - \frac{\varepsilon_s n_i d_{ox} w}{\varepsilon_{ox} N_d \tau_g} \tag{5}$$

We can neglect the second term in (5) assuming that

$$\frac{dU}{dt} >> \frac{q n_i d_i w}{\varepsilon_{ox} \varepsilon_0 \tau_g} \tag{6}$$

The correct choice of dU/dt allows for the use of only the first term in (5) to determine a non-equilibrium depletion width (w) in the MOS capacitor at each time. Solving (5) with the condition that a non-equilibrium depletion width $w(t) = 0$ at $U = U_1$, a simple equation for $w(t)$ is obtained:

$$w(t) = \left[\frac{2\varepsilon_0 \varepsilon_s}{q N_d} \left(U(t) - U_1 \right) \right]^{1/2} \tag{7}$$

Taking into account (1) and (2) for $U(t)$, the dependence on time for $w(t)$ for both half periods is determined as:

$$w(0,T)=\left(\frac{2\varepsilon_0\varepsilon_s\Delta U}{qN_d}\right)^{1/2}\left(\frac{t}{T}\right)^{1/2}$$
$$w(T,2T)=\left(\frac{2\varepsilon_0\varepsilon_s\Delta U}{qN_d}\right)^{1/2}\left(\frac{2T-t}{T}\right)^{1/2} \quad (8)$$

The filling of the potential well by thermo-generated carriers continues until the time at which this well is completely filled by minority carriers. At that moment, the value of $w(t)$ will decrease down to zero at the time $t = t_x$, and the capacitance leads to the value of C_{ox} as shown in Fig. 1.

The generation time (τ_g) may be obtained from (9) for the charge balance at $t = t_x$:

$$C_{ox}\Delta U\frac{2T-t_x}{T}=\frac{qn_iAw_0}{\tau_g}\left[\int_0^T\left(\frac{t}{T}\right)^{1/2}dt+\int_T^{t_x}\left(\frac{2T-t}{T}\right)^{1/2}dt\right] \quad (9)$$

where

$$w_0=\left(\frac{2\varepsilon_0\varepsilon_s\Delta U}{qN_d}\right)^{1/2}$$

After integrating, the equation for τ_g is:

$$\tau_g=qn_iw_0A\frac{4T^2-\left(2/T^{1/2}\right)\left(2T-t_x\right)^{3/2}}{3C_{ox}\Delta U\left(2T-t_x\right)} \quad (10)$$

III. EXPERIMENTAL RESULTS

The experimental data used for the determination of the generation lifetime with this novel method are shown in Fig. 2. The value obtained for the generation lifetime τ_g according to (10) is 517 ± 40 µs using the results obtained experimentally for $2T$ = 1.964 s, ΔU = 17.31 V, t_x = 1.932 s, $n_i = 5.1\times10^9$ cm^{-3} (at the measured temperature of 15.5 ºC). The parameters of the MOS capacitor with 60/70 nm SiO_2/Si_3N_4 oxide, and aluminum gate, are A = 0.06 mm^2, C_{ox} = 1.9 nF, ε_s = 11.8, ε_{ox} = 4.7, and $N_d = 2\times10^{12}$ cm^{-3}.

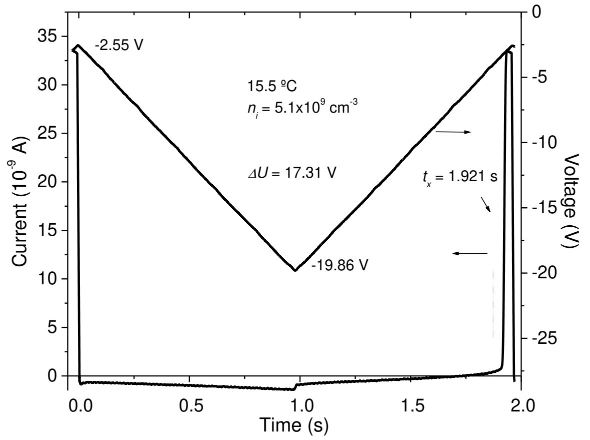

Fig. 2. Experimental data used for the determination of the generation lifetime with the proposed method.

We can clearly identify two sources of error when τ_g is determined using this method: 1) the precise knowledge of the majority carrier concentration (for the determination of w_0, and 2) the precise determination of t_x.

IV. DISCUSSION

In order to validate the proposed method, we must compare our presented results with those obtained using other methods. We show this comparison with those results obtained using two well-known methods for the determination of the generation lifetime. The most common is the Zerbst method for a pulsed MOS capacitor [3], and a τ_g = 510 ± 30 µs is obtained from the linear part of the Zerbst Plot shown in Fig. 3, using (11) without considering surface generation.

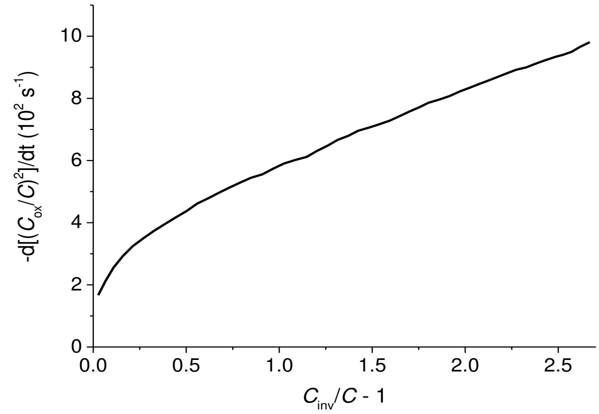

Fig. 3. Zerbst Plot from data of *C-t* response of a pulsed MOS capacitor.

$$-\frac{d}{dt}\left(\frac{C_{ox}}{C}\right)^2=\frac{2n_i}{\tau_{g,eff}N_d}\frac{C_{ox}}{C_{inv}}\left(\frac{C_{inv}}{C}-1\right) \quad (11)$$

The current-capacitance technique [1] presents an advantage in comparison with the Zerbst technique [3]; in this case it is not necessary to precisely know the majority carrier concentration in the substrate. Thus, according to the current-capacitance technique, the value of τ_g in the absence of surface generation can be obtained from the next dependence:

$$\frac{I}{\left[1-C(t)/C_{ox}\right]}=\frac{q\varepsilon_0\varepsilon_sn_iA^2}{\tau_g}\left(\frac{1}{C(t)}-\frac{1}{C_{inv}}\right) \quad (12)$$

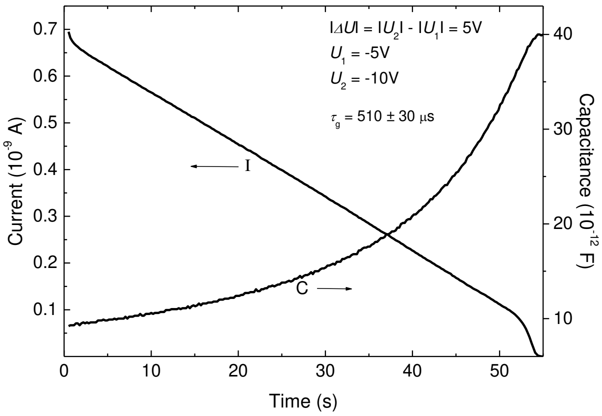

Fig.4. *I-t* and *C-t* characteristics of the MOS capacitor measured simultaneously.

Where C_{inv} is the saturated inversion capacitance measured at high frequency. The *I-C-t* characteristics at 100 kHz are shown in Fig. 4.

In order to use (12) to obtain the generation time, we use the experimental data to generate the plot shown in Fig. 5; from the linear part we extracted τ_g = 517 ± 15 µs.

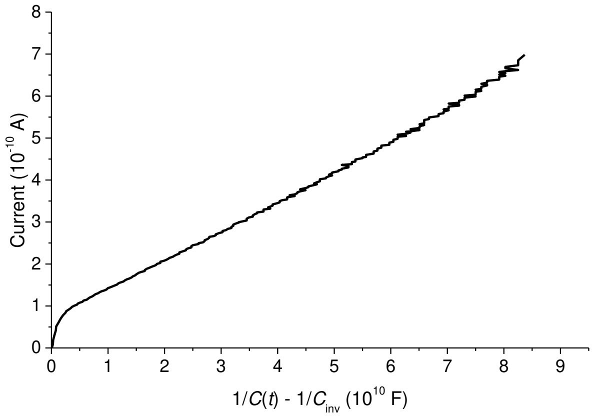

Fig. 5. Re-plotted data from Fig. 4 used to determine the generation time from the linear part, according to Equation (12).

Thus, one can see that the proposed method using a triangular sweep voltage to determine the generation time in MOS capacitor presents a good agreement with those results obtained by using other most common techniques.

We have used τ_g instead of its effective value τ_{eff} [1] in (8-10) because our MOS capacitor was designed in order to minimize additional effects due to surface generation in the gate perimeter. Furthermore, in this proposed method, the generation lifetime has been estimated with the capacitor initially operating in strong inversion in order to prevent the influence of the generation effects at the $Si/SiO_2/Si_3N_4$ interface under the gate electrode.

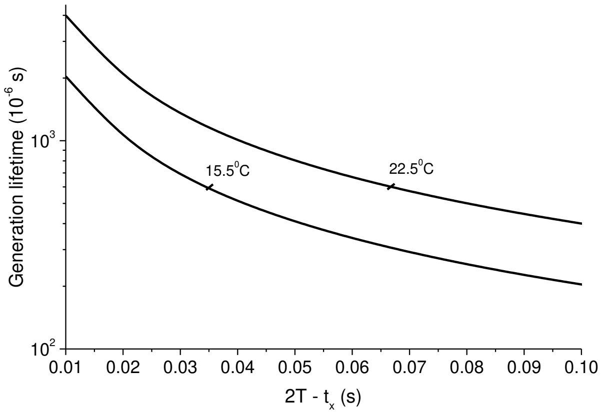

Fig. 6. Dependence of the generation time on the value of ($2T$ - t_x); the period $2T$ for the triangular voltage and ΔU are 2 s and 10 V, respectively.

The method using a triangular sweep voltage can be used, for instance, as a simple tool for "express monitoring" when a fast/easy determination of τ_g is necessary to control technological processes. The generation time can be determined easily from express measurements observed directly on a digital oscilloscope, and using a function generator operating under fixed parameters of the MOS capacitor and the triangular bias such as those shown in Fig. 1. Once the value of ($2T$-t_x) has been determined, it is easy the monitoring of τ_g via the graphical dependence of the generation time on ($2T$-t_x) according to (8). Fig. 6 shows an example of such dependence that has been used in our processes at different values of the intrinsic carrier concentration that depends on temperature.

Conclusions

It can be stated that the results presented in this work for obtaining the carriers generation lifetime, using a very simple and non expensive method, delivers values close to those obtained with more complicated techniques. This new method is proposed for monitoring the generation lifetime for processing devices based on high resistivity silicon substrates.

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