Low Power Full Adder Implementation Based on Pass Transistor Technology

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Abstract— *Addition is a fundamental for all the arithmetic operation, it is mainly used in digital signal processing architecture and microprocessor. The sum module is the core of arithmetic operation, like addition, subtraction, multiplication, division. The aim of the project is design of full adder having low power consumption and low power delay. In this project, a new hybrid 1-bit full adder is designed using both CMOS and pass transistor logic, for the purpose of reducing the no of transistors. It consists of three modules such as two XOR module and one MUX module. It is used to improving power delay product (PDP). This can be implemented by using the software Tanner EDA.*

Keywords— CMOS logic,MUX module, Pass transistor logic,Power delay product, Tanner EDA XOR module.

I. INTRODUCTION

The process of creating thousands of transistors are combined to a single integrated chip is a very large-scale integration. The microprocessor is one of the VLSI device. Using low power components with low power design is even more valuable. Battery power and its functionality are the requirements of the low power components. The VLSI designers concern with area, performance cost and also power as secondary of the design.Due to increase in growth in computing devices only power is considered. The motivations for reducing power consumption differ application to application. The source of power consumption in VLSI are

1) switching power
2) short circuit power
3) static power consumption.

The scaling supply voltage and capacitance are used to reduce the power consumption of VLSI circuit. With the reduction in supply voltage, problems of small voltage swing, insufficient noise margin and leakage current starts to instigate. The complementary pass transistor logic, Transmission gate logic, static and dynamic CMOS logic the full adders are designed.Hybrid technologies are used for designing the full adders in more than one different style. The improvement in power, delay and layout area was obtained using this logic style.

II. EXISTING FULL ADDER

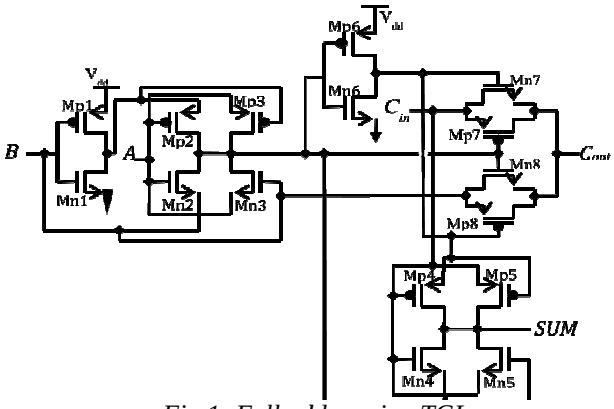

Fig.1: Full adder using TGL

In this both CMOS logic and transmission gate logic are used to design 1-bit full adder. The full adder circuit is divided into three modules. Module 2 is the XNOR module it generate sum signal and module 3 generate the carry signal.

The inverter is formed using transistors Mp1 and Mn1 generate B, which is used to implement the controlled inverter using the transistor pair Mp2 and Mn2. Output of this inverter is XNOR of A and B. It has voltage degradation problem which is eliminated using two pass transistors Mp3 and Mn3. PMOS (Mp4, Mp5, Mp6) transistors and NMOS (Mn4, Mn5, Mn6) transistors are form the second stage XNOR module to realize the complete sum function. In this circuit the output carry signal is implemented by the transistors Mp7, Mp8, Mn7, and Mn8. The input carry signal propagates through a transmission gate (Mn7 and Mp7), in order to reduce the overall carry propagation path significantly. The use of strong transmission gates (Mn7, Mp7, Mn8, and Mp8) areresponsible for reduction in propagation delay of the carry signal.

III. PROPOSED FULL ADDER

The Pass-Transistor Logic (PTL) is used to implement circuits designed for low power applications and its design and analysis procedures were reported. Perform the logic operation using only one PTL network, which providing small number of transistors and less input load in NMOS network. The short-circuit energy dissipation

are eliminated by using VDD to GND path. Due to low power consumption these circuits providing a non-full voltage swing at the output node.

To keep full voltage swing operation fewer transistor count and lower power consumption are more difficult. Due to the threshold loss problem, the output voltage swing are degraded in PTL. By using multiple of threshold voltage, the high voltage is deviated from VDD. The power is consumption due to reduction in voltage swing, but leads to slow switching in the cascaded operation such as ripple carry adder. The circuit malfunction is caused due to degraded output in low operation.

1 3T XOR GATE:

A formal design procedure, which are used for realizing a minimal transistor CMOS pass network XOR cell is presented. When the power supply voltage is very small then within the certain bounds, the new cells can be operate reliably and during initial step design it is given to sizing of the MOS transistor. Using the new XOR cell, a low transistor count full adder cells are presented. A PTL based 3-transitors XOR and XNOR circuits presented in full output voltage swing and has better driving capability.

An XOR/XNOR function with low circuit complexity can be achieved with only 3 transistors in PTL. The output voltage level in input combinations has the saving in transistor count. The low power 3 transistor XOR circuits is called as powerless XOR and XNOR circuits is called as Groundless XNOR and consumes less power than other design. Based on pass transistors logic, the new CMOS XOR circuit is designed. To produce XOR and the complementary XNOR functions only 6 transistors are used. This circuits are providing full voltage-swing andnegligible static power dissipation. The reduction in device count is the main advantages of this newly formed circuit.

2 XOR FULLADDER:

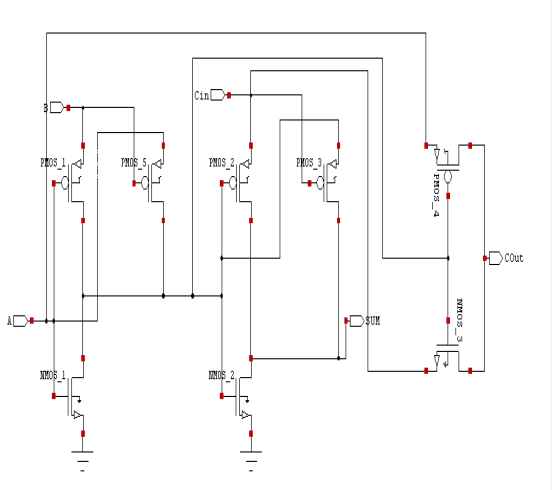

Fig.2: Full adder using PTL

The robustness against voltage scaling is the advantage of complementary CMOS. The XOR-XNOR based full adders realization is used to explain the above formed logic.

Hybrid full adder has been designed using PTL with the intermediate XOR-XNOR and output is improved. The hybrid full adder carry is a complementary CMOS logic style based MUX. By adding two series p-MOS and two series n-MOS transistors the delay problem is reduced from 01 to 00 and 10 to 11 respectively. The additional transistors improves the power consumption of the full adder circuit and also increases the speed of the circuit.

The PTL is used with the XOR circuit to produce a sum of the adder circuit. The driving capability for cascading is improved and output invertor restores the output voltage. Here we are uses 26 transistor having full swing, logic balanced at low voltage level. Another hybrid designed full adder is a combination of low power transmission-gates and NMOS gates. A particular type of pass transistors logic circuit has XOR gate that consists of a PMOS transistor and an NMOS transistor, it was connected in parallel.There is no voltage drop at output node but the design of similar function requires twice the no of transistors.

A novel 8-transistors XOR-XNOR based Full adder circuit that generates both XOR and XNOR outputs simultaneously. This circuit generatesa full voltage swing at low supply voltage. The reported XOR-XNOR Full adder circuit is based on complementary pass-transistor logic it uses only one static inverter instead of using two static inverters.

The first half of the circuit consist of only NMOS pass transistors for the generation of the XOR and XNOR outputs. Between XOR-XNOR outputs the cross-coupled PMOS transistors are connected to avoid the threshold problem for all thepossible input combinations and also reduce short-circuit power dissipation. Because of the high mobility NMOS transistors and the fast differential stage of cross coupled PMOS transistors the circuit is inherently fast. It indicates the functioning of the XOR/XNOR circuit.

IV. EFFICIENT SOFTWARE

1 TANNER EDA

Tanner tool is used in analog, mixed-signal, RF and MEM ICs. This tool consist of fully integrated front end and back end tools. L-edit pro is a physical layout and verification system used to accelerate design cycles which leads to high performance. T-spice pro is HSPICE used as Tanner EDA's design entry and simulation system. It includes S-edit for schematic capture, T-spice for circuit simulation, W-edit for waveform probing.This tool suite is ideal for applications including Power Management,

Life Sciences Biomedical displays, Image Sensors, Automotive, Aerospace, RF, Photovoltaic, Consumer Electronics and MEMS.

V. EXPERIMENTAL RESULT

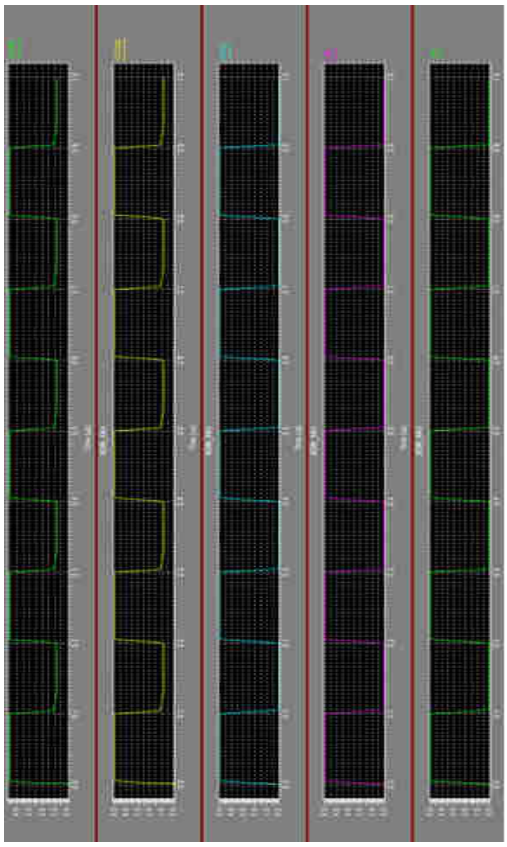

Fig.3: Output for PTL circuit

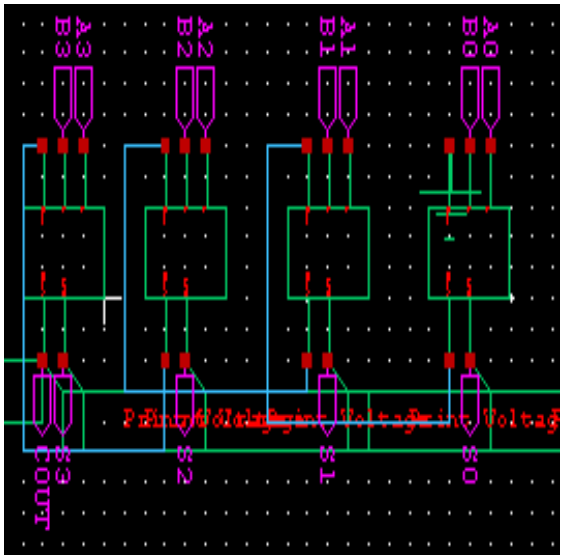

Fig.4: Ripple carry adder using PTL

Table.1: Power delay output

Design	Average power (W)	Delay (ns)	Transistor count
C-CMOS	1.5791µ	0.1269	28
Mirror	1.5701µ	0.1226	28
CPL	1.7598µ	0.0791	32
TGA	1.7619µ	0.2317	20
FA_DPL	7.34µ	0.254	22
FA_SRC PL	7.4µ	0.167	20
FA HYBRID TGL	5.182192e-003	4.6917 e-009	16
FA HYBRID PTL	4.396070e-007	3.2093 e-011	8

VI. CONCLUSION

Full adder is used in Digital signal processors (DSP) architectures and Microprocessor.It is used in the arithmetic logic unit (ALU), floating-point unit, and for address generation in case of cache or memory access. There is also an increasing demand for mobile electronic devices such as cellular phones, PDA's, and laptop computers requires the use of power efficient VLSI circuits. But major problem faced in this unit is power consumption and delay. By using this design we intend to reduce the power consumption and delay.

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