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An Innovative Approach of High Performance CMOS Based Current Conveyor-II for ASP Applications

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***Abstract*— The main purpose of the paper is to present a CMOS current conveyor circuit which is best suited for the implementation of low- voltage, low-power and high bandwidth circuits. To achieve the bandwidth of current transfer function the circuit can be operated for a power supply of fraction of volt which is of MHz range and a power consumption of milli-watt range. Firstly, a class A current conveyor circuit operating from a single supply of fraction of volt having a high voltage swing capability is discussed and then the same circuit is modified to work as a class AB with a low voltage power supply in the fraction of volt range, while maintaining the same voltage swing capability. The body effect causes the threshold voltage variation and the current circuit realization is insensitive to it, which minimizes the layout area and makes both the circuits a valuable addition to the analog signal processing applications. The proposed structure has the required performance in terms of a bandwidth with level 3 CMOS technology and it operates as a linear circuit which is established with the help of 0.3 µm simulation using the PSpice software. In the field of analog signal processing this proposed current conveyor circuit has many applications. At 0.2µm the proposed circuit operates satisfactorily with high performance with the desired applications. The desired properties and the performance of the proposed circuit are confirmed by the PSpice simulation with the modeled parameters.**

***Index Terms*— Current Conveyor (CC II), Analog Signal Processing, PSpice simulation, low votlage, high bandwidth, high performance, Current Mirror (CM), Operational Amplifiers (OA).**

I. INTRODUCTION

In the analog circuit designing the current conveyors and unity gain amplifiers are widely used, especially in the signal processing applications [1- 4]. The current controlled current source having unity gain amplification capability can be considered as the current conveyors (CC II). The circuit can be used in the realization of various sub-modules of the mixed analog processing applications of the systems [4, 5] and can also be used to take out the current flowing through a floating branch of a circuit. To obtain good dynamic swing at the output and high output so as to achieve a good cascadability, the high performance current mirror circuits are utilized in the CC-II. Most of the current conveyor circuits require high bias voltages as reported in the research sections of the various literatures. Thus, there always exists the requirement of the discussion of the CC circuits that can operate at low voltages and low currents. CC-I, CC-II and CC-III are the categorization of the basic current conveyor circuit [6, 8]. In the practical application of the analog signal processing, the CC-II has been proved to be more versatile as compared to the earlier one. The properties of the port of CC-II can be discussed as given below:

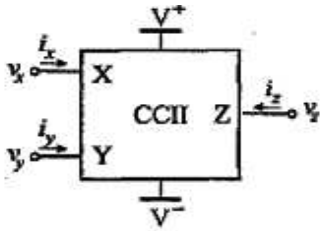

Fig. 1: Basic symbol of CC-II

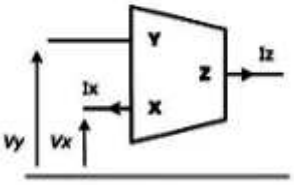

Fig. 2: Block approach of CC-II

$V_x = V_y$, $I_y = 0$, $I_z = \pm I_x$ … Basic Equations (1)

$$\begin{bmatrix} Iy \\ Vx \\ Iz \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} Vy \\ Ix \\ Vz \end{bmatrix}$$

CCII Node	Impedance level
X	Low (ideally 0)
Y	High (ideally ∞)
Z	High (ideally ∞)

Fig. 3: Performance Characteristics of CC-II

The matrix given above explains the port properties of a basic current conveyor structure, where Ix, Iy and Iz are the currents flowing in X, Y and Z nodes respectively. And Vx, Vy and Vz are the respective voltages in these nodes. Comparing it to CC-I, the innovation of this circuit can be represented by the absence of the current parameter in Y node, which owes to the high impedance. The signal applied to the Y node is almost equal to the X node and is given as:

$$\alpha = \frac{Vx}{Vy} = \frac{g_m r_o R_{XLOAD}}{1 + g_m r_o R_{XLOAD}} \quad (2)$$

$$\beta = \frac{I_z}{I_x} = 1 \quad (3)$$

Similarly, the ratio of the current Ix and Iz is discussed with the help of the equation (3). The following equations determine the various dominant parameters of a CC-II circuit.

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$$V_{in} = \sqrt{\frac{2I_{in}}{\beta_1}} + \Delta V_{th} + |V'| \quad (4)$$

$$R_{in} \approx \frac{1}{g_m} \quad (5)$$

$$R_{out} \approx \frac{g_m}{g_d}\frac{g_{m2}}{g_{d2}} \quad (6)$$

$$Z_y = \gamma W L C_{ox} \quad (7)$$

Where β, g_m, g_d, g_{m2} and g_{d2} are the dominant parameters that are used to discuss the performance of the CC-II circuit. And V' parameter is given by equation (8).

$$V' = nV_t \ln\left\{\frac{L_4}{W_4}\frac{I_{bias1}}{I_{DO4}}\right\} \quad (8)$$

II. THE BASIC CURRENT CONVEYOR CIRCUIT:

In the development of the analog and mixed signal processing applications the current conveyor circuits plays an important role using the CMOS approach [9, 13]. The CC-II is a three element device, which is basically defined with the help of three basic equations given.

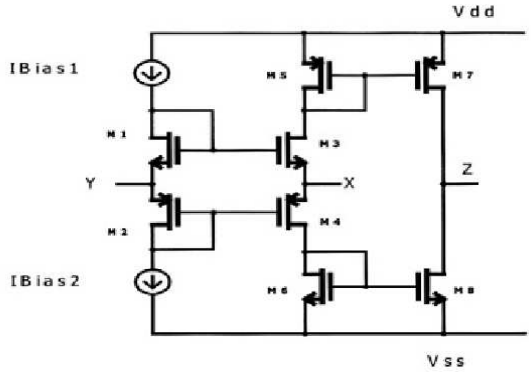

Fig. 4: Basic CC-II current approach using CM

$$Z_y = \gamma W L C_{ox} \quad (9)$$

$$Z_x \cong \frac{r_0 + R_{ZLOAD}}{1 + g_m r_o} \cong \frac{1}{g_m}, \text{ if } r_o >> R_{ZLOAD} \quad (10)$$

$$Z_z = r_0 + (1 + g_m r_o) R_{XLOAD} \quad (11)$$

In the design of analog signal processing circuits the CC-II act as the natural building block in the research field. It is observed that the signal applied to the y node (MOS gate) is almost equal to the signal obtained at the X node (source of the MOS). The ratio is approximately equal to 1 between the currents I_x and I_z and a constant parameter β determines it. The impedance behavior of the circuit at Y node can be determined as the gate capacitance of the MOS which is quite high as per the required parameters. Practically, γ being a constant parameter whose theoretical value becomes 2/3 in the saturation region, otherwise it is 1, W(width) and L(length) of the MOS transistor respectively, Cox is the unitary gain capacitance, and these can be related in the following manner i.e. [14]. From the fig. 4 CC-II circuit it is assumed that the two biasing currents are required to be equal. Also, that the product $g_m r_o$ value is much greater than unity and then the voltage characteristic of the circuit can be represented as:

$$\alpha = \frac{V_x}{V_y} = \frac{1}{1 + \frac{1}{(g_{m3} + g_{m4})\left(\frac{r_{03}}{r_{04}}\right)}} \cong 1 \quad (12)$$

With respect to the traditional implementations which utilize the commercial integrated circuits as the voltage OAs, CC-II based solution is used which reduces the system complexity. Many presentations and articles have witnessed the evolution of the first CC concept, demonstrating the universality of the element in the synthesis of almost all the active functions. To enhance the performance and the utility of the CCII block its evolution has regarded internal topology by maintaining the matrix characteristics. Firstly the CC-II was realized in bipolar technology as commercial products [14, 16]. The advent of MOS transistors has pushed the most of actual integrated solutions towards the use of CMOS technology having higher design simplicity and low power consumption particularly in low voltage portable system applications. CMOS devices suffers from many problems such as body effect, threshold voltage mismatch between nMOS pMOS and lower g_m values but its low cost especially for a standard technology represents a decisive feature towards its success and utilization. In the implementation of analog basic function the CC is widespread used. CCII-based circuits are always simpler in structure and more versatile, basically for the circuits which has high impedance current output capabilities with respect to commercial solutions with OAs [17, 18]. Furthermore, with the use of CCIIs, the heavy OA limitation of the constant gain-bandwidth product is definitely overcome.

III. PROPOSED CURRENT CONVEYOR CIRCUIT:

By using basic CC-IIs we can implement a number of analog applications such as voltage and current amplifiers, current differentiators and integrators, capacitance multipliers, impedance simulators and converters, bi-quadratic filters [19, 26], voltage-to-current and current-to-voltage converters, instrumentation amplifiers, oscillators and waveform generators, etc.. Many solutions are given in the literatures that were used in the past but now new possibilities along with high performance can be certainly considered for the future, especially at lower supply voltages and with more reduced dissipation. The implementation of the basic current conveyor holds an important aspect, having the operation and behavior of its non-ideal characteristics i.e. input and output real and imaginary parasitic impedances, current and voltage transfer functions. This approach leads us in the direction of an enhanced and modified model for the CC-II device [27, 29]. Moreover, the development of novel architectures able to implement analog functions with a lower number of basic elements can be of certain interest for the researchers with new fields of applications for the CC-II, i.e. the development of current-mode sensor interface circuits. The proposed circuit has four current mirrors, one biasing resistor and a translinear section which is composed of two current quasi-mirrors which are topologically similar to the current mirrors but they behave differently. The type of current mirror to be used depends on the application for which the circuit is designed and for which output voltages are needed in excess of the threshold voltage to operate properly. The basic current conveyor with simple current mirrors is implemented with a smaller number of transistors, influences the bandwidth of the circuit, i.e. it allows operation at higher frequencies. A smaller power supply voltage is needed for biasing of smaller no. of transistors and the power consumption is reduced. If all the CMOS transistors have matched characteristics and

infinite output resistances M6 and M8 have equal currents and gate-source voltages i.e.

$$i_{D6} = i_{D8} = I_{bias} \quad (13)$$
$$v_{GS6} = v_{GS8} \quad (14)$$

It implies that the desired performance of the circuit is achieved when i_y=0. The drain currents i_{D7}, i_{D9} are equal to the currents i_{D6} and i_{D8} when i_x=0. All drain currents of transistors in the translinear sections are equal to I_{bias}. Now when $i_x \neq 0$, then we can have

$$i_{D7} + i_X = i_{D9} \quad (15)$$

Since the complete current conveyor is symmetrical and all the CMOS transistors are matched then the following relationship holds for $i_x << I_{bias}$

$$i_{D7} \approx I_{bias} - \frac{1}{2} i_X \quad (16)$$
$$i_{D9} \approx I_{bias} + \frac{1}{2} i_X \quad (17)$$

With the use of the mathematical equations stated above, the proposed circuit behaves as a current conveyor circuit by fulfilling all the required conditions with the best possible performance and can also be utilized in the realization of the various analog signal processing applications.

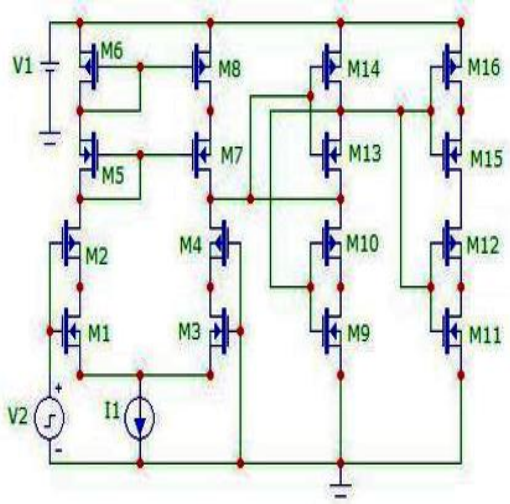

Fig. 5: Proposed Cascoded CMOS based CC-II circuit

IV. SIMULATION RESULTS:

The 0.2µm CMOS technology has been used to simulate the proposed CC- II circuit for level 3 parameters. The proposed circuit performance has been discussed in this simulation on the basis of transient analysis, dc analysis of the current conveyor circuit and performance or noise analysis, with the use of modeled parameters. Fig: 6 show the transient analysis of the proposed circuit with the desired performance. It exhibits that according to the theoretical concepts, this circuit exactly replicate the input with the accepted level of delay and with a minimum possible deterioration of the desired signal. Fig: 7 show the performance analysis of the circuit with respect to the gain and the phase analysis to the desired limits. And the fig: 8 show the dc analysis of the circuit, with the input signal replication at the output of the system. The noise performance of the circuit was evaluated and the noise gain was found nearly zero. The proposed structure's power consumption increases marginally from its rated value.

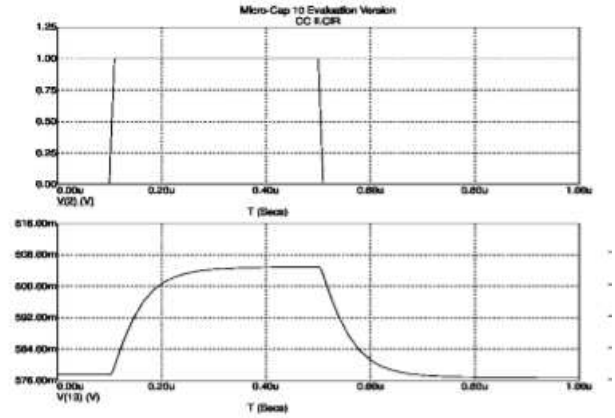

Fig. 6: Transient Analysis of CC-II

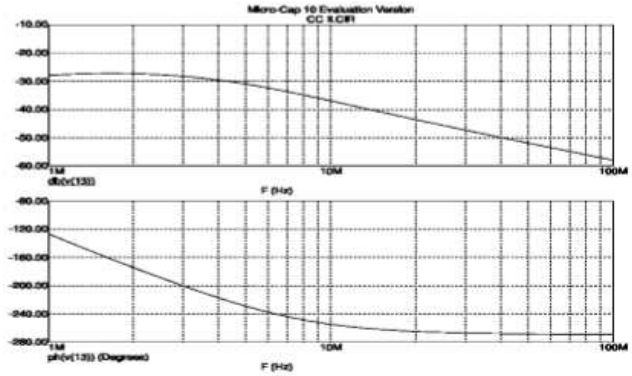

Fig. 7: Performance Analysis of CC-II circuit

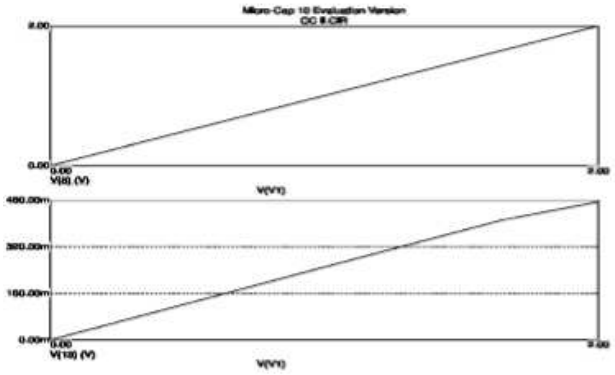

Fig. 8: DC analysis of the CC-II circuit

V. CONCLUSION:

In this paper, the authors have presented the overview of an innovative high performance current conveyor circuit that is capable of operating at low voltages. The proposed CC-II in the paper is capable to be operated at 1.0 V and exhibits a power dissipation of 3mW having a bandwidth of 60 MHz. The range of the input current extends from -300 pA to 300 pA. This structure could be easily modified to function as CCI, CCII or CCIII. The various algorithms of the signal processing use mathematical functions which can be generated using the application of this circuit. This CMOS based cascoded CC-II circuit realizations forwards a circuit that provides a rail to rail swinging capability having excellent linearity. No compensating capacitors are required by the circuit so, they have a wide bandwidth which is independent of the gain. The given circuits operation is insensitive to the threshold voltage variation which is the result from the body effect. PSpice simulations which are based on the level-3 parameters obtained through CMOS are in total support with

the expected results. The proposed CC-II circuit has better features and performance than the traditional ones.

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