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High Performance Sense Amplifier based Flip Flop Design using GDI Technique

Priyanka Sharma

Assistant Professor, Department of Electronics and Communication, Swami Keshvanand Institute of Technology Management & Gramothan, Jaipur, India

Abstract— *In this paper, a new approach is taken to design sense amplifier based flip-flop (SAFF) to improve performance of this device which is most frequency used in memory devices. With this, problem of cross coupled SR latch in existing SAFF (NAND latch) is removed. The new flip-flop uses a new output stage latch topology using GDI technique that significantly reduces power consumption and has improved power-delay product (PDP). Various topologies along with their layout simulations have been compared with respect to the number of devices, power consumption, power-delay product, temperature sustainability in order to prove the superiority of proposed design over existing conventional CMOS-NAND design. The simulation has been carried out on Tanner EDA tool on BSIM3v3 45nm technology.*

Keywords— CMOS digital integrated circuits, flip-flops, GDI Technique, latch topology, low power, Power-Delay product, memory elements, Dual edge triggered flip flops, sense-amplifier, Tanner EDA.

I. INTRODUCTION

This paper is based on the analysis of basic memory elements called flip-flops. In order to achieve a design that is both highly efficient and high performance, it is necessary to take care while designing these memory elements i.e flip-flops and latches. We have proposed a new SAFF using GDI technique in which GDI latch has been used. First we modified existing design by applying GDI technique to flip-flop stage, then a new design is introduced by applying GDI technique in the sensing stage of flip-flop. Simulation results proved that proposed design is better than modified and existing SAFF.

II. SENSE AMPLIFIER BASED FLIP-FLOP

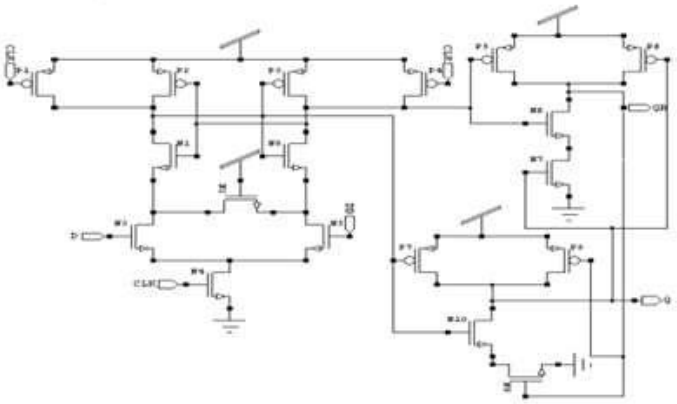

Fig.1: Schematic of existing SAFF

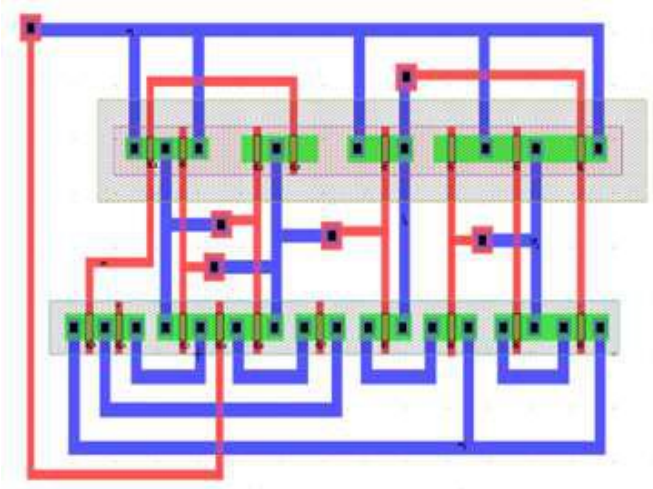

Fig.2: Existing SAFF layout

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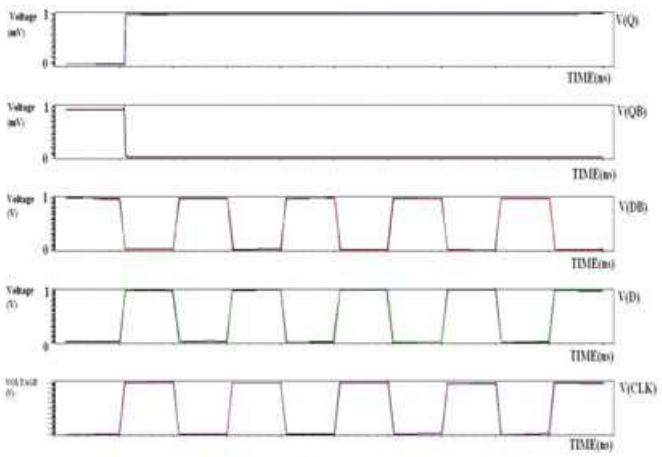

Fig.3: Waveforms of Existing SAFF

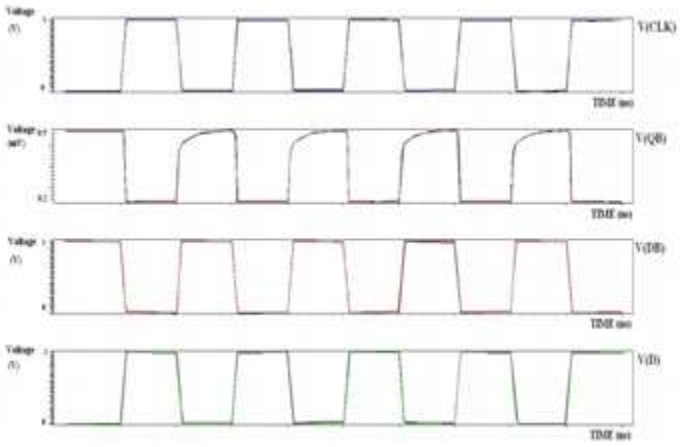

Fig.6: Waveforms of modified SAFF

Modified SAFF:

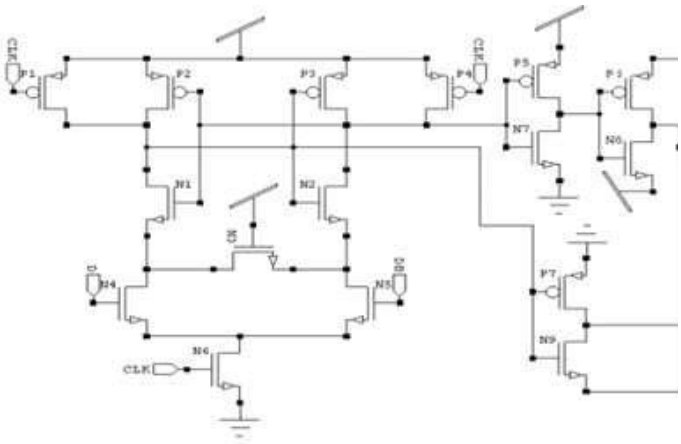

Fig.4: Schematic of modified SAFF

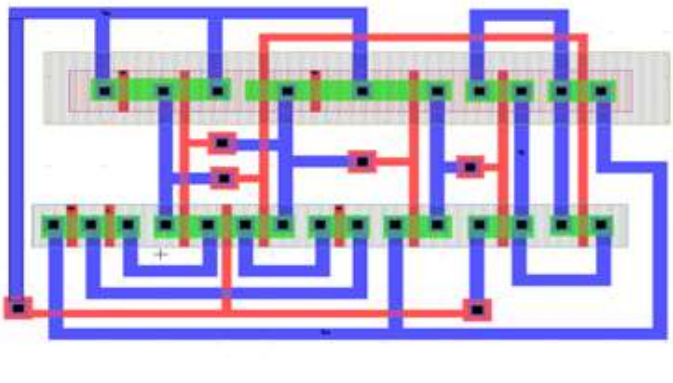

Fig.5: Modified SAFF layout

III. PROPOSED SAFF

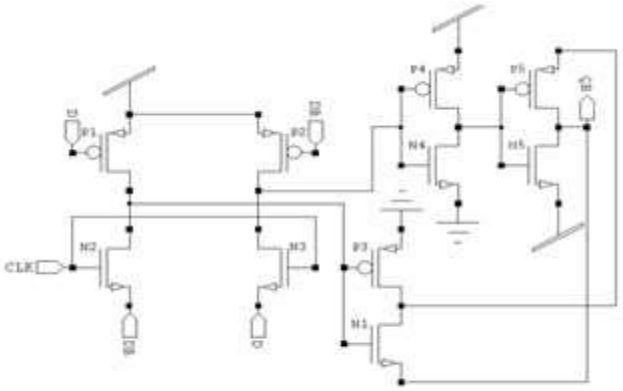

Fig.7: Schematic of proposed SAFF

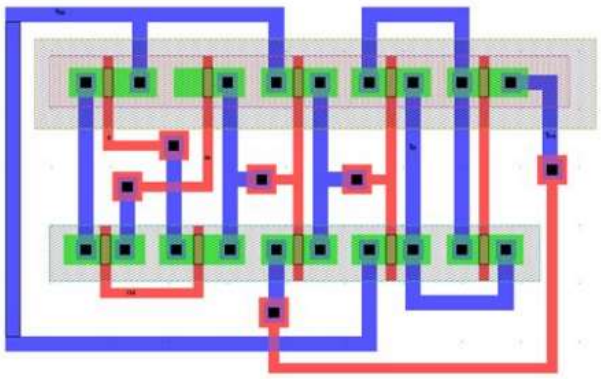

Fig.8: Proposed SAFF layout

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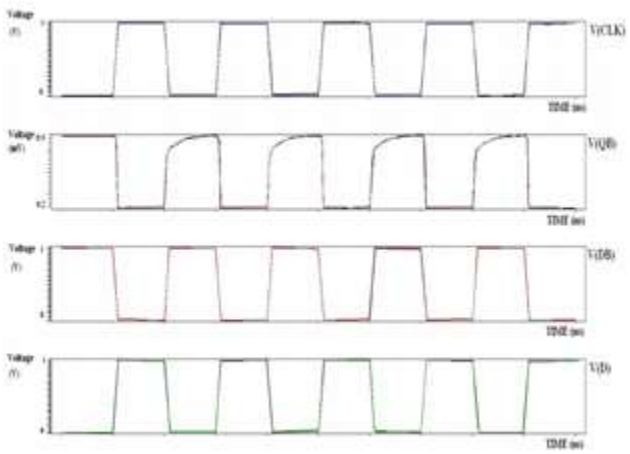

Fig.9: Waveforms of proposed SAFF

Table.I: PDP values of different topologies corresponding to supply voltage

Supply Voltage(volts)	PDP Existing	PDP Modified	PDP Proposed
1.25	11.219978 e-014	87.41100225 e-015	89.042391 e-015

Both modified and proposed designs are dual edge triggered while existing design is single edge triggered.

As given in Table I, power-delay product of modified and proposed designs is equivalent but less than existing design. Hence, proposed and modified design is superior over existing design in terms of PDP. Total number of transistors in existing, modified and proposed SAFF is 18, 16 and 10 respectively. Area overhead of proposed design is least.

IV. SIMULATION AND COMPARISON

Simulation Environment: All the circuits have been simulated using BISM 3V3 45nm technology on Tanner EDA tool. To make the impartial testing environment, all the circuits have been simulated on the same input patterns. All experimental results for temperature, frequencies and capacitance are carried out at VDD=1.25 V

Pre-layout Simulation Comparison:

Performance comparison of both modified and proposed SAFF Design with existing SAFF Design:

In this paper, various parameters are compared in order to prove the superiority of modified and proposed design over existing SAFF. Fig.10-11 show power consumption variation over different operating ranges of temperature, supply voltage respectively. Delay variation with supply voltage is shown in the Fig.12.Fig 13 shows the variation of power consumption versus frequency. Fig.14 shows delay variation over different operating range of frequency. Fig.15-16 show power consumption and delay variation over different values of output load capacitance. Fig. 10 shows that power consumption of existing SAFF is largest among modified and proposed SAFF. Power consumption of modified and proposed SAFF is almost comparable. Fig. 11 shows that as supply voltage is increasing, power consumption of modified design is least while it is highest for proposed design. Hence, modified design is power economical according to pre-layout simulations in terms of power consumption. There is a continuous decrease in delay with rise in supply voltage and this variation is same for all designs as shown in Fig.12. Fig.13 shows that power consumption is almost increasing with respect to frequency. In this case, power consumption is least for proposed design while it is highest for modified design.Fig.14 shows that delay variation is same for all of the three designs with respect to frequency. Fig.15 shows that power consumption across output load capacitance is highest for existing SAFF, while it is least for proposed SAFF and almost comparable with modified design. As capacitance value increases, delay for all the three designs remains constant. This behavior is shown in Fig.16.

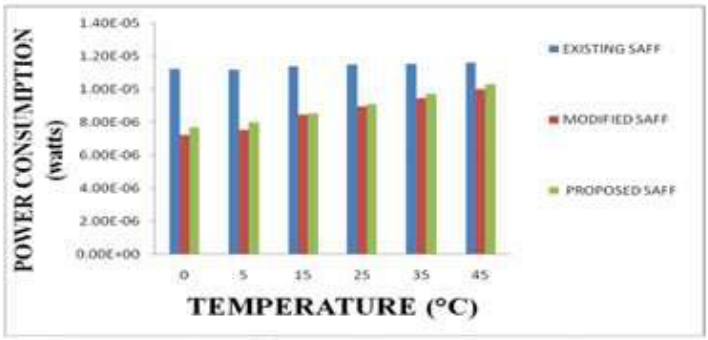

Fig.10: Power consumption variation over different operating ranges of temperatures at VDD=1.25V

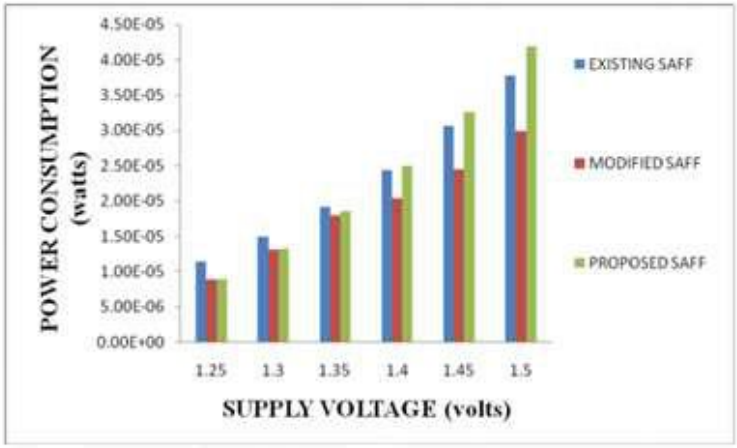

Fig.11: Power consumption variation over different operating ranges of supply voltages at VDD=1.25V

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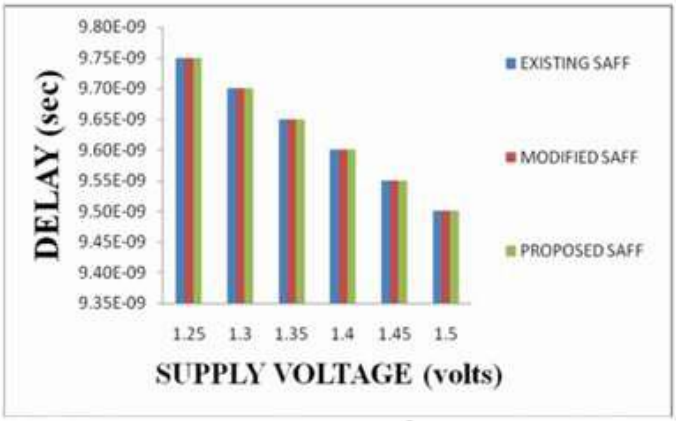

Fig.12: Delay variation over different operating ranges of supply voltages at VDD=1.25V

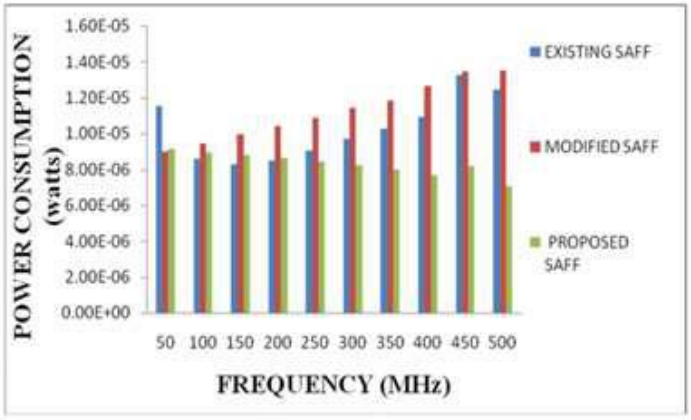

Fig.13: Power consumption variation over different operating ranges of frequencies at VDD=1.25V

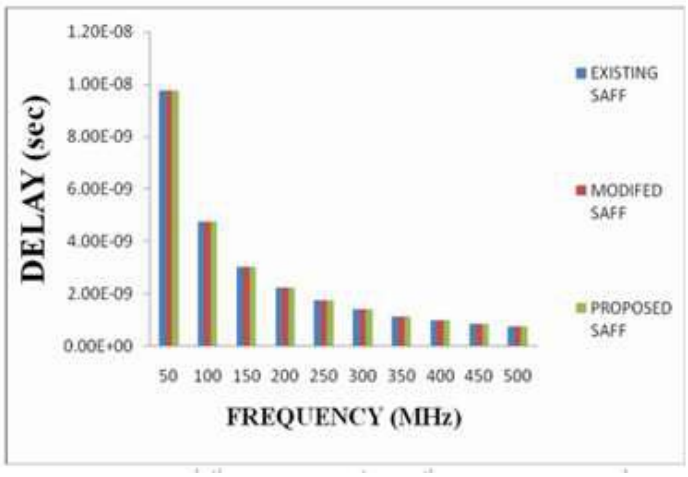

Fig.14: Delay variation over different operating ranges of frequencies at VDD=1.25V

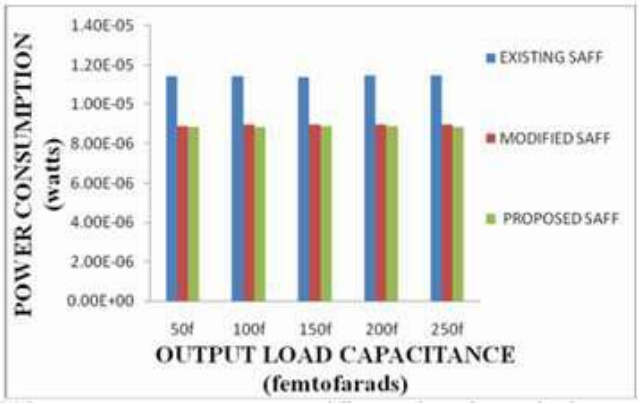

Fig.15: Power consumption variation over different values of load capacitances at VDD=1.25V

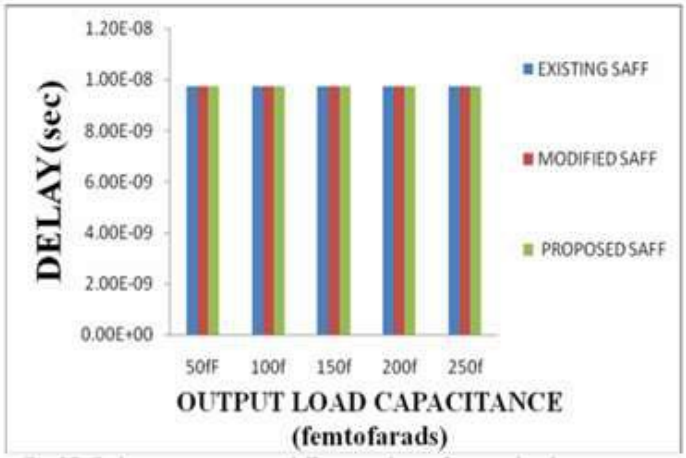

Fig.16: Delay variation over different values of load capacitances at VDD=1.25V

V. CONCLUSION

In this paper, a particular D flip-flop configuration known as Sense amplifier based flip-flop (SAFF) is presented. Existing SAFF is compared with modified SAFF and proposed SAFF. Modified SAFF and proposed SAFF designs are proved to be better than existing SAFF. On the basis of simulation results, power-delay product of modified SAFF is least at 1.25 volts. Hence, proposed design proved to be better as compared to modified design in terms of power consumption, PDP as well as parasitic capacitance.

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REFERENCES

[1] A. Chandrakasan and R. Brodersen, Low-Power CMOS Design, IEEE Press, 1998,pp. 233-238.

[2] N. H. Weste and K. Eshragian, Principles of CMOS VLSI Design: A Systems Perspective, 2nd ed. Reading, MA: Addison-Wesley, 1994.

[3] M. Shoji, Theory of CMOS Digital Circuits and Circuit Failures. Princeton, NJ: Princeton Univ. Press, 1992.

[4] N. Nedović and V. G. Oklobdzija "Dual-edge triggered storage elements andclocking strategy for low-power systems," IEEE Transaction on VLSI Systems,vol. 13, pp.577-590, May 2005.

[5] C. K. Tsai, P. T. Huang, and W. Hwang, "Low power pulsed edge triggered latches design," 16th VLSI Design/CAD Symposium, 2005.

[6] Goh Wang Ling, Yeo Kiat Seng, Zhang Wenle and Lim Hoe Gee," A Novel Static Dual Edge-Triggered Flip-flop for High-Frequency Low-Power Application", A Novel International Symposium on Integrated Circuits, 2007. ISIC '07. pp.208-211

[7] S. H. Unger and C. J. Tan, "Clocking schemes for high-speed digital systems," IEEE Trans. Comput., vol. C-35, Oct. 1986.

[8] V. Stojanovic and V. G. Oklobd˘zija,"Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems," IEEE J. Solid-State Circuits, vol. 34, pp. 536–548, Apr. 1999.

[9] V. Stojanovic´, V. G. Oklobd˘zija, and R. Bajwa, "A unified approach in the analysis of latches and flip-flops for low-power systems,"in Proc. Int. Symp. Low-Power Electronics and Design, Monterey, CA, Aug. 10–12, 1998, pp. 227–232.

[10] H. Partovi et al., "Flow-through latch and edge-triggered flip-flop hybrid elements," ISSCC Dig. Tech. Papers, pp. 138–139, Feb. 1996.

[11] C. Svensson and J. Yuan, "Latches and flip-flops for low power systems,"in Low Power CMOS Design,A. Chandrakasan and R. Brodersen, Eds. Piscataway, NJ: IEEE Press, 1998, pp. 233–238. [12]M. Pedram, Q. Wu, and X. Wu, "A new design of double edge triggered flip-flops," in Design Automation Conference, Asia and South Pacific,pp. 417-421, 1998.