Simulation of TI-SEPIC Converter for BLDC Motor Drives

S.Sathiyamoorthy[1], Dr. M.Gopinath[2]

[1]Research Scholar, Department of EEE, St.Peter's University, Chennai, India
[2]Professor, Department of EEE, Dr.N.G.P.Institute of Technology,Coimbatore, India

Abstract— *Power Factor Correction (PFC) is one of the research areas in the field of power electronics due to the enormous power required in various industrial applications. In this work, a SEPIC converter with the Tapped Inductor model which is operated in Discontinuous current Conduction Mode (TI-SEPIC-DCM) is proposed for a BLDC Drive. The proposed TI-SEPIC-DCM also improves the voltage gain with the help of voltage multiplier cell and charge pump circuit. It also helps in attaining the ZVS and ZCS, which results in higher switching frequency range and reduction in size reduction. Moreover, a third order harmonic reduction control loop is also proposed to attain a better third order harmonic elimination. The proposed work has been simulated using MATLAB simulink and the results are also validated.*

Keywords— Power Factor Correction, TI-SEPIC – DCM, BLDC, Total Harmonic Distortion.

I. INTRODUCTION

The various power supplies having active power factor correction (PFC) methods are required for a wide range of applications for the purpose of biomedical , automobile and various industrial applications. All the above applications are expected to satisfy the industry standards like the IEC 61000-3-2. Furthe, it is highly recommended to adopt to new Industry standards such as 80 PLUS initiative. Several papers have been presented in the literature for providing a solution for the case of single-stage power factor correction (PFC) and other integrated topologies [1-7]. These solutions have been useful in providing cost-effective approach in attaining both high PFC and rapid output voltage control.

The Various PFC rectifiers make use of boost converter at their front end. Boost converter has several benefits like power factor correction capacity and simple control [8]. The low voltage applications such as telecommunication or computer industry requires an extra converter or an isolation transformer for stepping down the voltage. But, the traditional boost coverter has lesser efficiency because of considerable losses in the diode bridge [1]. In addition to the above , boost converters are worst affected by high inrush current that in turn increases the cost incurred in the safety . In order to reduce the losses due to the presence of the full bridge, number of bridgeless PFC rectifiers have been proposed for improving the rectifier power density. [2]-[5] through the soft switching methods.

The various types of non-boost bridgeless rectifiers are also presented in the literature duirng recent times [9]-[13]. A bridgeless PFC rectifier using SEPIC topology is introduced in [11]. The SEPIC topology consists of only a step up capability using boost transformer; An isolation transformer may also be used for stepping down the voltage, thereby leading to an increased cost and size of the rectifier. The Cuk converter topology is normally a converter with less efficiency, but it has few benefits, like isolation capability, step up or stepping down output voltage, constant load current and reduced electromagnetic emissions.

At the same time, a Single-Ended-Primary-Inductor Converterb(SEPIC) is a type of dc-dc converter that permits the potentil at its output to be presented less than or greater than or equal to that of its input. The SEPIC is controlled with the help of the duty cycle corresponding to the control switch. It has inherited the merits of having a true shutdown and non inverted output. There are more chances to obtain a high voltage gain using this converter. SEPIC converters have a significant applications in industries.This converter works at a pre-determined duty ratio and switching frequency.

Tapped Inductor (TI) type of converters are an another option, which provides simple circuit and less number of part count. The TI boost (TI-boost) converter [14] can accomplish much more gain than its fundamental counterpart simply by varying the the turn's ratio. TI can be introduced to other conventional dc–dc converters also. TI-flyback [15], TI-cascaded boost [15]; TI-SEPIC [16], [17] and TI-ZETA [18] topologies have been reported.

II. PROPOSED TI- SEPIC DCM CONVERTER FOR BLDC DRIVE.

The Control Loop c diagram of the proposed SEPIC converter with TI model operating in DCM (TI-SEPIC-DCM) is shown in Figure 1. This converter circuit includes a Diode Bridge Rectifier (DBR); an input inductor L_1, a main switch Q, a capacitor C_1. A voltage multiplier cell is added into the circuit, which includes C_M, D_M, a Tapped Inductor (TI) of L_p, L_s, and a charge pumping unit is added into the circuit, which includes C_2, D_1 and D_0, feeding an output filter capacitor,C_o, and a load R_L,. The Tapped Inductor's turn's ratio,n is given as,

$$n = N2/N1 \quad (1)$$

At this point, N_1 and N_2 are the primary and the secondary number of turns, respectively.

This converter is developed from the basic SEPIC topology [20]. The inductor L1 is swapped with TI in order to accomplish higher voltage gain. Additional gain is achieved through the process of applying a voltage multiplier cell. It also assists the proposed converter attaining Zero-Voltage switching and ZCS(Zero Current Switching) as well as ZVS(Zero Voltage Switching, which will improve the efficiency, and enables higher switching frequency and reduced size. It also has an extra advantage. In case if the switch,Q is turned on, the charge pump capacitor,C1 fastens the anode voltage of the output diode, Do, to ground. Thus the, the voltage stress of Do is free of the TI turns ratio and same is obtained as the output voltage. This lessens the switching losses of Do and is an additional benefit of this converter. In addition, this converter is also designed to operate in DCM to achieve almost UPF and low Total Harmonic Distortion (THD) of the input current. Since it is operated in DCM the control circuit becomes simpler because it uses only one voltage sensor in the circuit.

Control of proposed BL TI-SEPIC DCM converter

A. Front end converter control

The converter proposed which is working in DCM indicates a third-harmonic distortion in the input current, this current distortion is actually a function of the voltage difference existing between the input and the output voltage. Usually, the output voltage is raised for the purpose of reducing the third-harmonic distortion and for maintaining high power factor, though there is an increase in the semiconductors losses. The aim of minimizing the third-harmonic without any increase on the output voltage has led to the introduction of an open-loop control action.

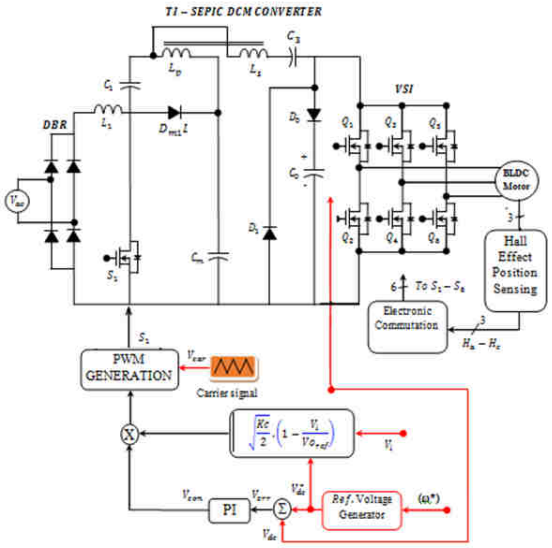

Fig 1: Control Loop Diagram of the Proposed Converter

A single voltage control loop (voltage follower approach) is used for the TI SEPIC converter which functions in DCM. A reference dc link voltage (V_{dc}^*) is produced as

$$V_{dc}^* = k_{volt} \times \omega^* \quad (3)$$

In which k_{volt} and ω^* refer to the corresponding motor's voltage constant and the reference speed.

The voltage error signal (V_{err}) is generated by having a comparison of the reference output voltage(V_{dc}^*) with the output voltage sensed (V_{dc}) as

$$V_{err} = V_{dc}^*(k) - V_{dc}(k) \quad (4)$$

Where k represents the kth sampling instant. This error voltage signal (V_{err}) is provided as input to the voltage proportional–integral (PI) controller for the generation of a controlled output voltage (V_{con}) as

$$V_{con}(k) = V_{con}(k-1) + k_p\{V_{err}(k) - V_{err}(K-1)\} + k_i V_{err}(k) \quad (5)$$

Where $k_p$and k_i refer to the respective proportional and integral gains of the voltage PI controller.

$$D(\omega t) = \sqrt{\frac{K_c}{2}} \cdot \sqrt{1 - \frac{V_{pk}.\sin(\omega t)}{V_0}} \quad (6)$$

Where, $K_c = \frac{8.P_0.L_{eq}.f}{V_{pk}^2}$

Only the output and input voltages are required for controlling the converter. In the same time, the rectified input voltage that is sensed (V_i) and the output voltage reference are applied to (4) for calculating the variation of duty-cycle for the third-harmonic reduction. The result from the PI output voltage controller and also the result from the

third-harmonic reduction are multiplied thus getting the converter duty cycle and then having the PWM signal generated which regulates the main switch S_1.

B. Control of BLDC motor drive

The electronic commutation of the BLDC motor contains the proper switching of VSI in such a manner that a symmetrical dc current is obtained from the dc link capacitor for 120◦ and then placed in a symmetrical manner at the centre of every phase. A Hall-effect position sensor is employed for sensing the rotor position with a span of 60◦ that is necessary for the electronic commutation of the BLDC motor.

Table.I: Switching states based on hall effect position signals

θ^0	HALL SIGNALS			SWITCHING STATES					
	H_a	H_b	H_c	S_1	S_2	S_3	S_4	S_5	S_6
NA	0	0	0	0	0	0	0	0	0
0-60	0	0	1	1	0	0	0	0	1
60-120	0	1	0	0	1	1	0	0	0
120-180	0	1	1	0	0	1	0	0	1
180-240	1	0	0	0	0	0	1	1	0
240-300	1	0	1	1	0	0	1	0	0
300-360	1	1	0	0	1	0	0	1	0
NA	1	1	1	0	0	0	0	0	0

The line current is obtained from the dc link capacitor whose magnitude depends on the dc link voltage that is applied, back electromotive forces, resistances, and self-inductance and mutual inductance with respect to the stator windings. Table 1 illustrates the various switching states of the VSI powering a BLDC motor on the basis of the Hall-effect position signals (*Ha − Hc*).

III. SIMULATION RESULTS

The performance of the proposed BL TI-SEPIC- DCM converter is simulated in a MATLAB / Simulink environment using the SimPower-System Toolbox. The performance of the proposed converter is evaluated for rated conditions to valuate the power quality indices obtained at ac mains.

Parameters such as supply voltage (V_s), supply current (i_{ac}), Switch S_1 current (i_{sw1}), Switch S_2 current (i_{sw2}), Dc link voltage (V_{dc}), Speed of the BLDC motor (N), Motor Torque (T_e), Stator Current (I_a), converter output voltage, output current and output powe V_{OUT}, I_{OUT} and P_{OUT} respectively. Moreover, power quality indices such as power factor (PF), Total Harmonic Distortion (THD) of supply current are analysed for determining power quality at ac mains.

A. Steady-State Performance

Figure 2(a)-(g) shows the proposed converter operates at rated Vac of (20 Vrms), rated speed of 1500 rpm and rated Torque of Te (1.2 Nm). Based on the above mentioned rated conditions, the corresponding response of the proposed converted is evaluated in the following waveforms. The stator current, Switch S_1 current and Switch S_2 current are maintained at the desired reference value as shown in Figures 2(e-g).

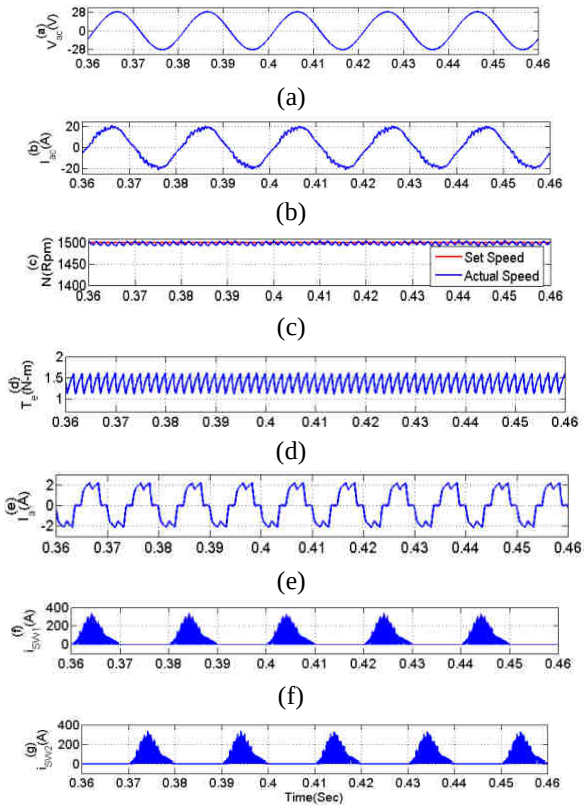

Fig.2(a)-(g): Steady State Responses of the Converter

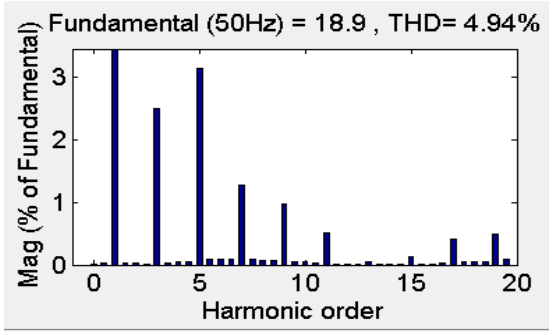

Fig.3: THD for the Proposed Converter

IV. CONCLUSION

This paper proposed an efficient PFC Converter for BLDC motor applications. The proposed TI-SEPIC-DCM for BLDC motor application. The results are simulated for dynamic varying conditions such as varying the speed of the BLDC motor. The converter results are obtained for the rated conditions.. It is clear that THD results are obtained for third order harmonic reduction with minimal THD (4.94%). Thus, the proposed converter results in near unity PF improvement through third order harmonic reduction for BLDC motor application.

REFERENCES

[1] A. A. Fardoun & E. H. Ismail, "Non-isolated Single Stage PFC Rectifier for Wide-Input Large Step-Down", International Journal on Power Electronics, vol. 2, no. 4, pp. 412-427, 2010.

[2] G. Moschopoulos and P. Kain, "A Novel Single-Phase Soft Switched Rectifier With Unity power Factor and Minimal Component Count," IEEE Trans. on Ind. Electron., vol. 51, no. 3, pp. 566-575, June 2004.

[3] Y. Jang and M. Jovanovic, "A Bridgless PFC Boost Rectifier with Optimized magnetic Utilization," IEEE Trans. on Power Electron., vol. 24, no. 1, pp. 85-93, Jan. 2009.

[4] L. Huber, Y. Jang and M. Jovanovic, "Performance Evaluation of Bridgless PFC Boost Rectifiers," IEEE Trans. on Power Electron., vol. 23, no. 3, pp. 1381-1390, May 2008.

[5] A. A. Fardoun, E. H. Ismail, Ahmad J. Sabzali and Mustafa A. Al-Saffar, "New "Real" Bridgeless High Efficiency ACDC Converter", 27th annual IEEE Applied Power Electronics Conference (APEC), Orlando, pp. 317-323 Feb. 2012.

[6] M. Brkovic and S. Cuk, "Input current shaper using Cuk converter," in Proc. Int. Telecommun. Energy Conf., 1992, pp. 532–539.

[7] E. Mahdavi, M. and H. Farzanehfard, "Bridgeless SEPIC PFC Rectifier With Reduced Components and Conduction Losses" IEEE Trans. Ind. Electron., vol. 58, no. 9, p. 4153- 4160, 2011.

[8] A. Sabzali, E. H. Ismail, M. Al-Saffar and A. A. Fardoun, "A New Bidgless PFC Sepic and Cuk Rectifiers With low Conduction and Switching Losses", 8th International Conference on Power Electronics & Drives Systems, PEDS 2009, pp550-556, November 2009.

[9] M. Brkovic and S. Cuk, "Input current shaper using Cuk converter," in Proc. Int. Telecommun. Energy Conf., 1992, pp. 532–539.

[10] E. Mahdavi, M. and H. Farzanehfard, "Bridgeless SEPIC PFC Rectifier With Reduced Components and Conduction Losses" IEEE Trans. Ind. Electron., vol. 58, no. 9, p. 4153- 4160, 2011.

[11] A. Sabzali, E. H. Ismail, M. Al-Saffar and A. A. Fardoun, "A New Bidgless PFC Sepic and Cuk Rectifiers With low Conduction and Switching Losses", 8th International Conference on Power Electronics & Drives Systems, PEDS 2009, pp550-556, November 2009.

[12] A. A. Fardoun, E. H. Ismail, A. J. Sabzali and M. A. AlSaffar, "A Comparison between Three Proposed Bridgeless Cuk Topologies and Conventional Topologies for Power Factor Correction," IEEE Transactions on Power Electronics,Vol. 27, no. 7, pp. 3292-3301, July 2012.

[13] M. R. Sahid, A. H. Yatim, and N. D. Muhammad "A bridgeless Cuk PFC converter", IEEE Applied Power Electronics Colloquium (IAPEC), pp. 81 – 85, 2011.

[14] Vazquez, N., et al., 2007. "The tappedinductor boost converter". in Proc. IEEE Int. Symp. Ind. Electron., pp. 538–543.

[15] Liang, T. J. and Tseng, K. C., 2005. "Analysis of integrated boost-flyback step-up converter," Proc. Inst. Electron. Eng.: Elect. Power Appl., 152(2), pp. 217–225.

[16] Lin, B. R., and Hsieh, F. Y., 2007. "Soft-switching zeta-flyback converter with a buck–boost type of active clamp". IEEE Trans. Ind. Electron., 54(5), pp. 2813–2822.

[17] Kim, K. D., et al, 2011. "Improved non-isolated high voltage gain boost converter using coupled inductors". in Proc. IEEE Int. Conf. Electr. Mach. Syst., pp. 20–23.

[18] Axelrod, B., and Berkovich, Y., 2011. "New coupled-inductor SEPIC converter with very high conversion ratio and reduced voltage stress on the switches". in Proc. IEEE 33rd Telecommun. Energy Conf., pp. 1–7.