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Parametric Reliability of Low Power Adiabatic SRAM

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Abstract— *This paper presents our attempt to recover back energy that is stored in the bit lines and in the cell and reused it by a phenomenal technique of energy recovery known as adiabatic principles. By the application of this adiabatic driver the loss of energy to the ground during '1'to'0' transition in SRAM is reduced to a greater degree. In this paper the performance of the conventional 6T SRAM circuit is compared with the performance of the Adiabatic 6T SRAM. In the adiabatic SRAM good high degree of power reduction is reported. By applying the aforementioned technique same SRAM is investigated by varying technology. Another parameter such as delay and power delay product (PDP) is also been calculated for all the SRAM. All the circuits are simulated in HSPICE and delay is calculated using Cosmo scope.*

Keywords- SRAM, Adiabatic logic, Low power, delay, SNM, WTP, sense amplifier.

I. INTRODUCTION

Today we enjoy great low power consumer devices is the direct impact of much phenomenal development of the VLSI technology. As in late 1970s Moore stated a law that in every eighteen month the number of transistor in the chip becomes double. Therefore, to meet the requirement of the portable appliances various low power techniques had been used [1]. For this designer explore new approaches to the design of VLSI circuits. Energy recovering (adiabatic) logic is a new promising approach, which has been originally developed for low power digital circuits [2-4].

In this paper we concentrated only on the design of Static memory using adiabatic logic. As it is known that memory consumes maximum power in any device, maximum efforts have been given to reduce as much as power consumption in memory.The structure of the paper is as follows, Section 1 is the introduction, section 2 contain the overview of SRAM, section 3 contain the overview of Adiabatic logic, section 4 contain the design of conventional and adiabatic SRAM, section 5 shows all the result related to SRAM such as power, delay, PDP. Finally section 6 contains the summary and conclusion of the paper.

II. SRAM OVERVIEW

Static memory (SRAM) cells use a latch composed of cross-coupled inverters to store data as shown in Fig. 1.

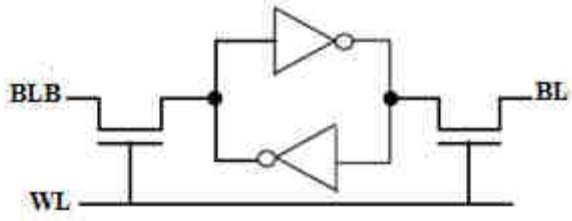

Fig. 1: SRAM cell with two cross coupled inverters.

The schematic for static RAM Cell is shown in Figure 2. Essentially, the data is latched at the cross-coupled inverters. The bit-lines are complementary and are input to the I/O of the inverters. Thus, the value is latched during a write and maintained as long as power is available.

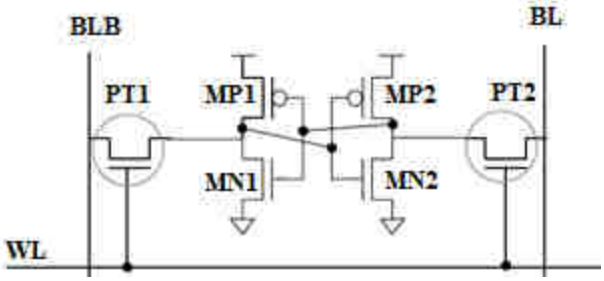

Fig. 2: Schematic of 6T SRAM

The working of the SRAM is simple and easy to understand. 6T SRAM cell consist of 6 transistor, two pull up transistor (MP1, MP2), two pull down transistor (MN1, MN2) and two pass transistor (PT1, PT2). The gate of pass transistor is controlled by the word line input. Whenever the word line is high the BL and BLB are connected to the cell hence the cell can be read out or write in from the bit lines. When the WL is off there is no reading or writing is performed by the cell, hence the cell will be in the hold state.

For successful writing to be done in the cell there must be a write driver which monitor the presence of data and allow that data to be written into the cell. This write driver is simple a AND gate whose input are write enable and data.

When reading is to be done the write enable of the write driver is switch off so that writing is not performed. Reading is carried out with the help of sense amplifier.

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There is a column transistor which is on by the read enable input when the reading is carried out by the sense amplifier. Sense amplifier is a differential amplifier which senses the difference between the voltages in BL and BLB. It is also very important to mention here that before reading is to begin the BL and BLB are to be pre charge to the certain level of voltage so that both the lines would have same voltage. This pre charge is done by the pre charge circuit.[6]

III. ADIABATIC LOGIC OVERVIEW

Adiabatic is a Greek word which means "impassable" is basically defined in thermodynamic principle of state change with no loss or gain of heat. This adiabatic principle is explained with the help of switching activity done in electrical circuit.

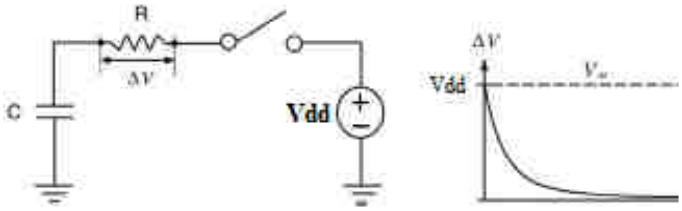

Fig 3: RC network with switch

Fig. 3 shows the energy dissipation during a switching transition in conventional CMOS circuit. The circuit shows the transition of the switch from LOW to HIGH which as a result the capacitor charges and discharges. When the switch is open the Vdd supply is not connected to the capacitor hence the capacitor is not charged. When the switch is closed, voltage Vdd is applied and current start flowing through R, this as result charges the capacitor to voltage Vdd. The energy taken from the power supply is C.Vdd ^{2,} but half of that 1/2CVdd^2 is stored in C and the rest half is dissipated in R. [5]

Now, consider the circuit and current waveform shown in Fig. 4. Here notice that, instead of using a fixed power supply as in the previous case we use a time varying power supply. By this slow transition of the supply voltage the charging and discharging time of the capacitor is greatly increased.

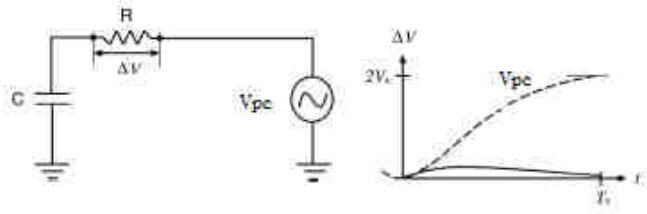

Fig. 4: Adiabatic logic with sinusoidal power supply

As it is well known that the energy loss during charging and discharging is given by the following formula.

$$E = \frac{RC}{T} C.Vdd^2 \quad \ldots\ldots\ldots\ldots (1)$$

Where, R = Resistance

C = Load Capacitance

T = Charging and Discharging time

Vdd = Supply Voltage

From the equation 1 it is clear that the as the charging time of the capacitor is increased the energy loss in the circuit is reduced. This is the reason that here a time varying power supply is used instead of a fixed power supply.

IV. DESIGNING 6T SRAM

In this paper our main focus is in the 6T static random access memory.

4.1 Conventional 6T SRAM

Fig. 5 shows the conventional 6T SRAM circuit. The basic architecture of 6T SRAM consist of a pre charge circuit, write driver, SRAM cell, Column transistor and sense amplifier.

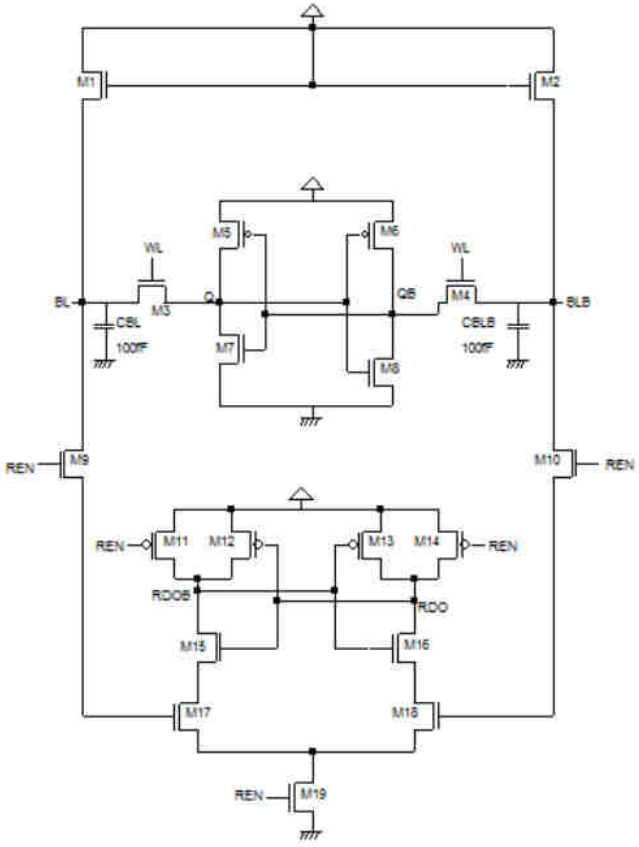

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Fig 5: Conventional 6T SRAM with Precharge and Sense amplifier

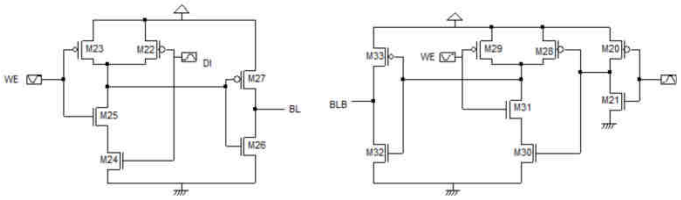

Fig 6: Write Driver circuit for conventional 6T SRAM

Pre charge circuit comprises of transistor M1 and M2.Figure 5 shows the RAM cell with the bit-line conditioning circuit that charges the bit lines using n-type transistors. Both bit lines are charged to VDD-Vth, where Vth is the threshold voltage of the precharging nmos. It is also possible to use p-type transistors for the precharge transistors, and this would pull up the bit lines to VDD instead of to VDD-Vth. However, it will take longer to pull down the bit lines. Thus, using n-transistors improves the speed of the RAM.[7-9]

Fig 5 shows the SRAM cell which comprises of transistor M3-M8, out of which transistor M3 and M4 are the access transistor and are operated by the word line, the data from BL and BLB are written into the Q and QB when the WL is ON. Similarly the data from Q and QB are read though the bit lines.

The transistor M9 and M10 are the column transistor which allows bit lines data to be read by sense amplifier. The primary objective of a sense amplifier in an SRAM array is to amplify a small bitline differential voltage swing to a full-swing logic output.This kind of sense amplifier is easy to implement and operates with reasonable speed and power consumption.

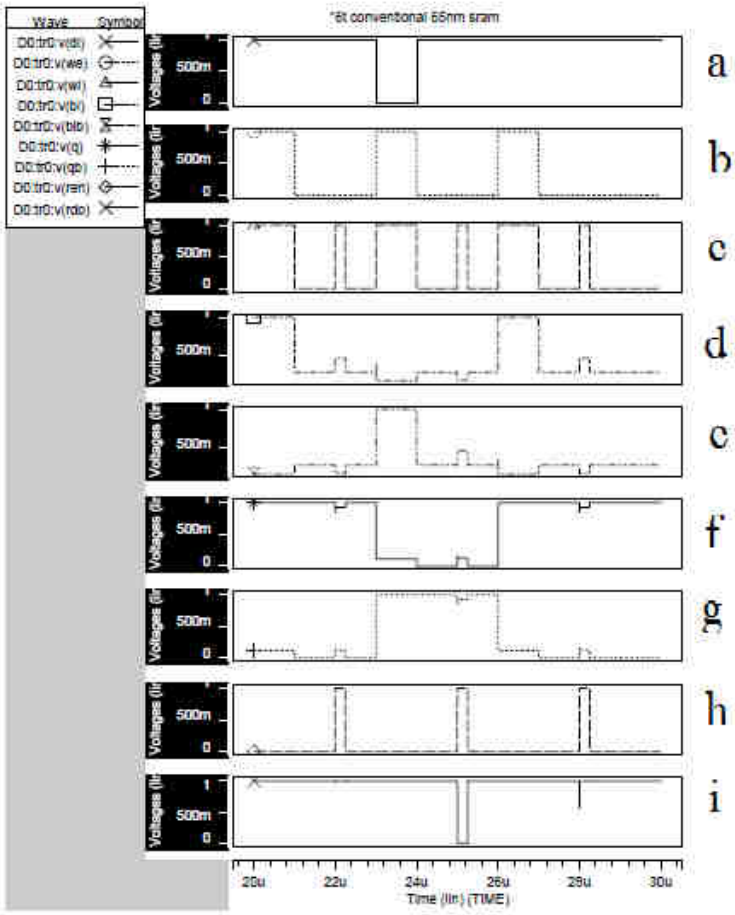

Fig. 7: Simulation Waveform of conventional 6T SRAM

Fig. 6 shows the write driver circuit which are implied on both the bit lines. The write driver is typically an AND gate whose two input are Write Enable (WE) and Data (DI). The output of the AND gate is applied to the bit line. Whenever the WE is on the data DI is travel to the bit lines. Otherwise the data is disconnected from the bit lines.

Figure 7 represent the simulation waveform of the conventional 6T SRAM. Simulation is done in HSPICE tool. Inputs are represented as DI, WE, WL, REN in the waveform a, b, c and h respectively. These inputs are taken in such a way that in 10um time duration the 3 times writing, reading and hold operations are performed. As a consequence of the given input the writing output are represented by the BL, BLB, Q and QB in the waveform d, e, f and g respectively.The reading output is shown by the RDO signal shown in waveform 'i'.

This can be seen that when the input WE and WL is high the data DI is written over Q and QB. Both Q and QB are the complimentary to each other. In the case of reading one can see that when WL and REN are ON and WE are OFF, reading takes place. For very small interval only reading is

carried out. The output of the sense amplifier is taken out from RDO.

All the transistor width and length are taken according to the normal consideration. For n-type transistor the ratio of width and length is taken 1:1, except the precharge transistor whose ratio is taken as 2:1. For p-type transistor the width is taken either twice, thrice or four times the length of the particular transistor. There are three variant of 6T SRAM are simulated according to the technology variation (180nm, 130nm, 65nm). The dc voltages applied to SRAM are 2.0v, 1.5v and 1.0v for 180nm, 130nm and 65nm respectively. The output waveform are seen almost similar in all the variants, the only changes occur in the power and delay parameter. All the results are shown in next section.

4.2 Adiabatic 6T SRAM

Normally conventional SRAM consume more power for the satisfactory working. To reduce this power requirement author uses the most promising approach of adiabatic technique in SRAM circuit. It is seen that when an input logic 1 is written over the cell, the value remain high until and unless a low logic is overwritten over that particular cell. Consider that you want to write logic 0 into the cell and previously the data present in the cell is 1. Now to overwrite the new value one has to pass all the previous data (i.e. logic 1) towards ground so that the new data in the cell is logic 0. This discharge of the high potential towards ground is just wastage of energy. This wastage can be recovered with the help of energy recovery technique.

Basically the concept behind the recovery of energy is that the access voltage which has to be grounded to overwrite new data is not grounded instead of that it is return back to the power supply. Here it is important to mention that the power supply used over here is not the fixed power supply, instead of that author uses the time varying power supply. This time varying power supply is known as power clock.

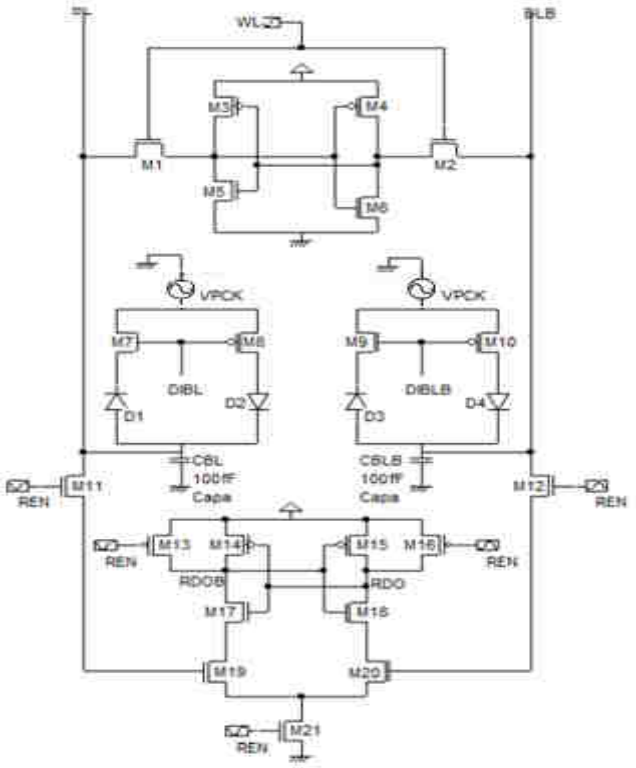

Fig. 8: Circuit diagram of adiabatic 6T SRAM

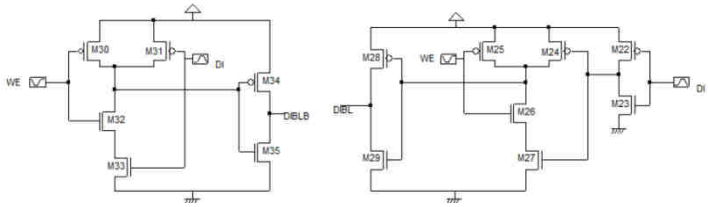

Fig. 9: Write driver circuit for Adiabatic 6T SRAM

Here time varying power supplies are triangular pulse, trapezoidal pulse or the sinusoidal pulse. By using the triangular power clock differently the power is reduced but the delay is increased very much. Hence by using the sinusoidal or trapezoidal power clock delay can be reduced. Author uses the sinusoidal power clock which recovers the very high power without much increase in delay.

Figure 8 shows the adiabatic SRAM with the sense amplifier. In this the extra circuit used is the circuit made with help of two diode and two transistors. When the input DIBL is low then the transistor M8 is ON and the sinusoidal power clock VPCK is flow through the diode D2 and it charges the capacitor CBL which is connected to the BL. Similarly when the DIBL is high transistor M7 is ON the high charged stored in the capacitor flow back through diode D1 towards power clock VPCK. Other working of the sense amplifier is similar to that of the conventional SRAM.

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In figure 8 it is seen that the pre charge circuit is absent in the adiabatic circuit. The reason behind the absence of the pre charge circuit is that, while reading operation both the bit lines are to at the same potential so when write enables (WE) is OFF then both the output of the write driver (i.e. DIBL and DIBLB) is 0. Hence the transistor M8 and M10 are and high voltage flow from diode D2 and D4. Hence both the bit lines (BL and BLB) are at the high potential.

The simulation of adiabatic SRAM is done using HSPICE in 180nm, 130nm and 65nm technology. Fig. 10 shows the simulated waveform of the adiabatic SRAM. All the parameter is same as that in conventional SRAM circuit. The frequency of the power clock is taken 1 MHz.

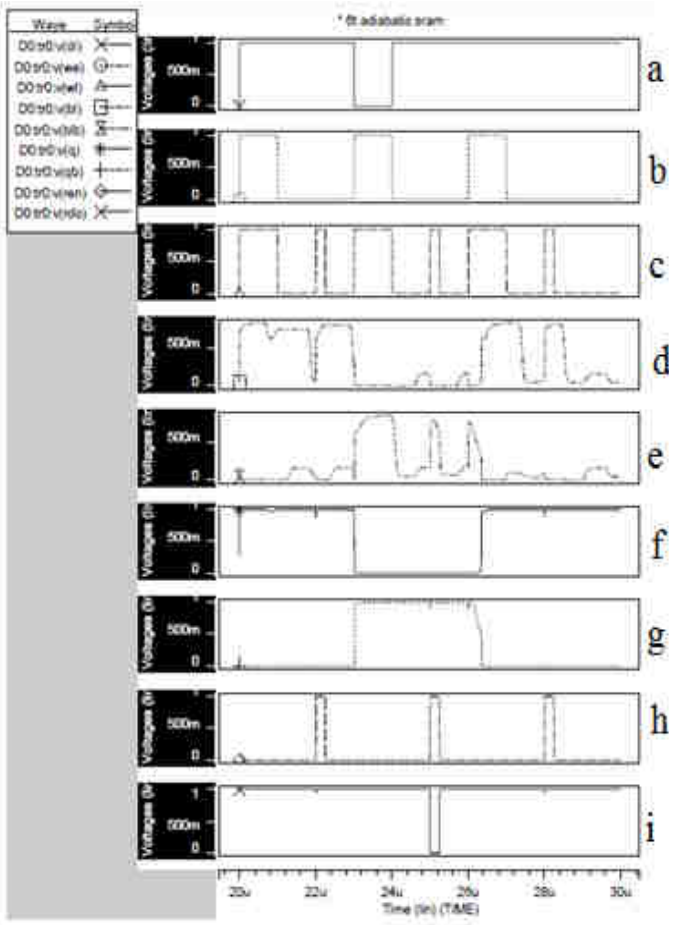

Fig. 10: Simulation Waveform Adiabatic 6T SRAM

V. SIMULATION RESULTS

In the following section we describe the simulation result based on the above simulation. We have designed an adiabatic SRAM using HSPICE simulator with different technology model. Based on that the result obtained are shown below

5.1 Power dissipation

Power dissipation is the major factor that we dealt with adiabatic logic. Adiabatic technique helps us in reducing the power consumption in any circuit. Table 1 show the average power obtained from the HSPICE simulation of the 6T SRAM in different technology.

Table 1

Average Power (µm)	Technology Variation		
	65nm	**130nm**	**180nm**
Conventional 6T SRAM	50.212	191.23	495.84
Adiabatic 6T SRAM	0.882	6.302	15.207

Figure 11 shows the graphical view of table 1.

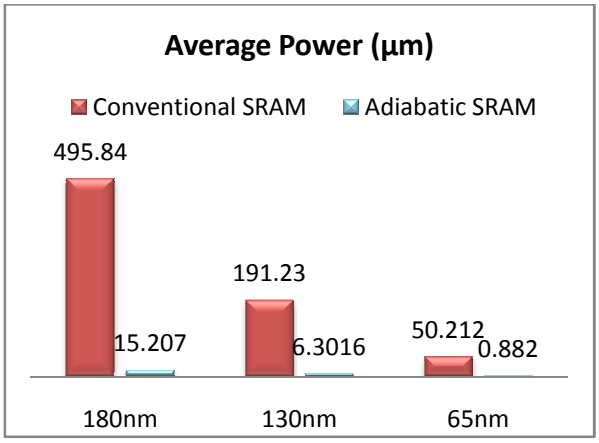

Fig. 11: Average power (µm) in different technology for conventional and adiabatic SRAM.

Table 2

Technology	Percentage of power reduction in adiabatic SRAM
65nm	98.24%
130nm	96.70%
180nm	96.93%

Table 2 shows the percentage of power reduction in adiabatic SRAM as compared to the conventional SRAM.

5.2 Delay

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Delay calculation is the prominent section of any digital circuit. As it well known that while decreasing the power consumption in any circuit by applying any low power technique, the delay in the circuit is increased. This delay must be not so much high that it would affect the working of the normal circuit. Delay calculation is bit easy by using the Cosmo scope tool.

Table 3: Write Delay

Technology Variation	Write Delay (ps)	
	Conventional SRAM	Adiabatic SRAM
65nm	724.59	4856
130nm	659.20	52053
180nm	590.45	1190.3

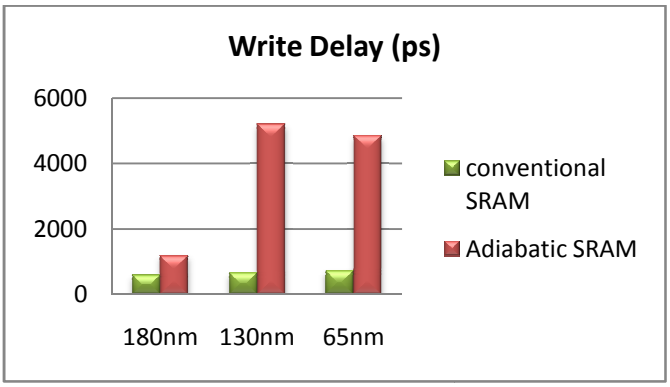

Fig. 12: Write Delay for conventional and adiabatic SRAM.

Table 4: Read Delay

Technology Variation	Read Delay (ns)	
	Conventional SRAM	Adiabatic SRAM
65nm	1.165	2.322
130nm	0.550	1.2057
180nm	0.405	1.396

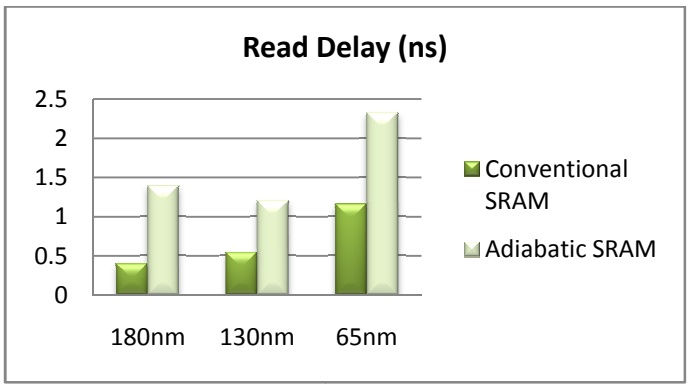

Fig. 13: Read delay for conventional and adiabatic SRAM.

Table 3 and 4 shows the write delay and read delay for the conventional and adiabatic SRAM. The Write delay for the adiabatic SRAM is increased as compared to the conventional SRAM. The write delay is in the picosecond range. Figure 12 shows the write delay in graphical view. Figure 13 shows the read delay in graphical view.

5.3 Power Delay Product (PDP)

The power delay product (PDP) is the product of the power and the delay of the SRAM. Table 5 shows the power delay product of the conventional and adiabatic SRAM.

Table 5

		Write PDP(fJ)	Read PDP(fJ)
65nm	Conventional	36.4	58.2
	Adiabatic	4.28	2.04
130nm	Conventional	126.0	105.3
	Adiabatic	32.8	7.59
180nm	Conventional	292.0	200.7
	Adiabatic	18.1	21.22

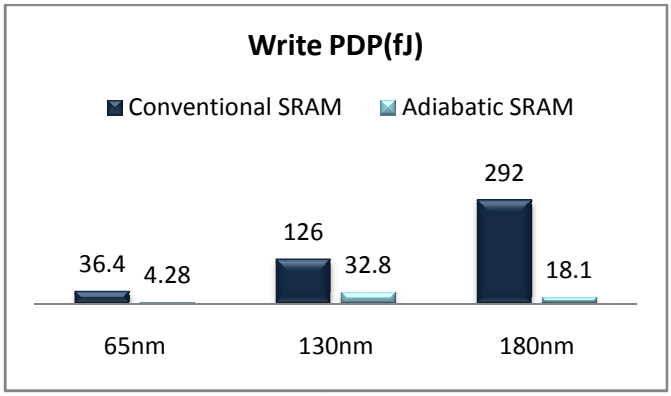

Fig. 14: Write PDP for conventional and Adiabatic SRAM

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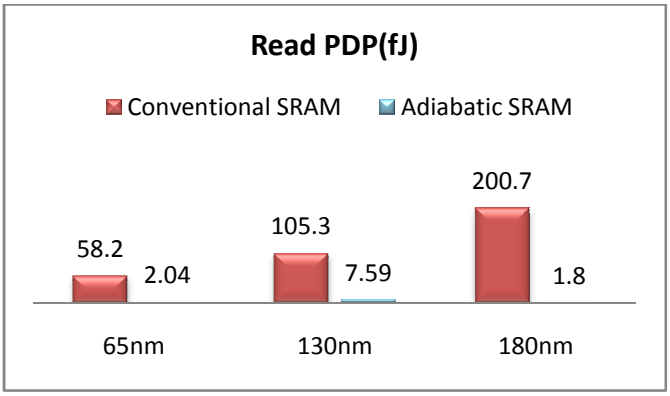

Fig. 15: Read PDP for conventional and Adiabatic SRAM

Figure 14 shows the power delay product of the write operation take place in conventional and adiabatic SRAM. Figure 15 represent the power delay product of the read operation take place in different technology in conventional and adiabatic SRAM.

Table 6

Technology	Percentage of Energy saving	
	In Writing	In Reading
65nm	88.24%	96.5%
130nm	73.96%	92.8%
180nm	93.8%	89.4%

Table 6 shows the percentage of energy saving by using adiabatic technique in 6T SRAM while reading and writing operation at different technology.

VI. CONCLUSION AND SUMMARY

The advantage of adiabatic logic is low-energy operation but the disadvantage is slower operation than CMOS. Therefore, the concrete application is a low-speed processor, not a high-speed processor. In this paper we presented a low power 6T SRAM based on the energy recovery technique.

The conventional SRAM and adiabatic SRAM are simulated using HSPICE in 65nm, 130nm and 180nm technology. Different results based on the simulation have been shown in section 5. We found that the average power reduction for whole SRAM circuit in 65nm technology is 98%, in 130nm technology is 96% and in 180 nm technology it is 96%.If we talk in terms of energy recovery take place in write operation is about 73% to 93% in different technology. Similarly in the case of read operation about 89% to 96% of the energy is recovered as compared to the conventional part.

As it is well known that the adiabatic logic provides delay in the circuit. This fact is proved in ourcircuit also. The write delay and read delay of the adiabatic SRAM is considerably increased as compared to normal SRAM. This is the main disadvantage of the adiabatic logic. But this delay is not so much high that it would affect the proper working of the circuit. Focusing on the fact that the reduction in power consumption and recovery of such a huge amount of energy makes this circuit configuration beneficial.

Here it is also important to notify that as we decrease the technology from 180nm to 65nm we found that the power consumption is also decreased. Here we have simulated only single cell of the SRAM and for that we have used single adiabatic circuit in bit lines. Even for building up large memory only single adiabatic circuit is used for one column, whether the column consist of hundreds of cell. This fact make the area of the proposed SRAM approximately same as that the conventional SRAM.

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