https://dx.doi.org/10.22161/ijaers.4.4.22 *ISSN: 2349-6495(P) | 2456-1908(O)*

Design of High Performance and Energy Efficient Explicit Pulsed Sense Amplifier Based Flip-Flop

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Abstract— *In this paper, we have presented a new design of explicit pulsed sense amplifier based flip-flop (SAFF) which gives high performance parameters. The most important factors need to be considered while designing efficient circuits are low power with less delay .Our proposed design attracted these performance parameters due to its design using GDI technique. Different topologies along with their layout simulations have been compared with respect to power consumption, delay and temperature sustainability in order to prove the superiority of proposed design. The simulation has been carried out on Tanner EDA tool on BSIM3v3 45nm technology.*

Keywords— Explicit pulsed SAFF, GDI Technique, latch topology, low power, delay, Power consumption, Dual edge triggered flip flops, sense-amplifier, Tanner EDA.

I. INTRODUCTION

With the increasing demand for high-performance and energy efficient memory devices, there is a lot of attraction in the design work towards meeting the above requirements. An explicit-pulsed flip-flop is used for critical paths due to its energy efficient feature. All simulations have been carried out on Tanner EDA Tool on BSIM3v3 45 nm technology. Using GDI technique, SAFF-GDI latch is simulated first ,there after we have modified it by adding explicit pulse to trigger it which is shown as explicit pulsed SAFF-GDI latch.

II. SAFF USING GDI TECHNIQUE

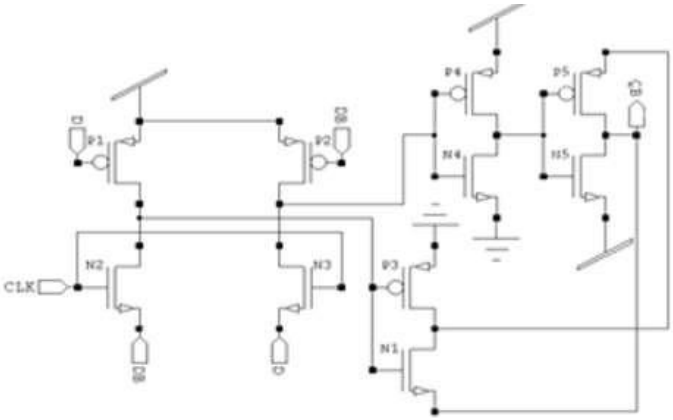

Fig.1: Schematic of SAFF-GDI latch

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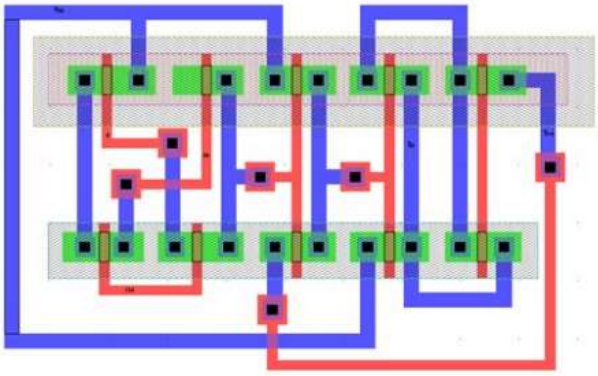

Fig.2: SAFF-GDI latch layout

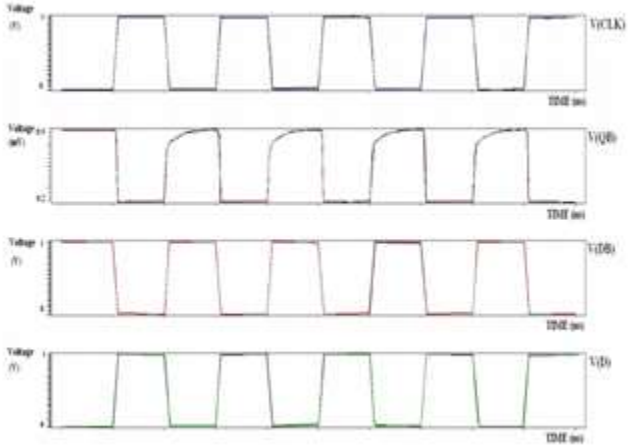

Fig.3: Waveforms of SAFF-GDI latch

Explicit pulsed proposed SAFF

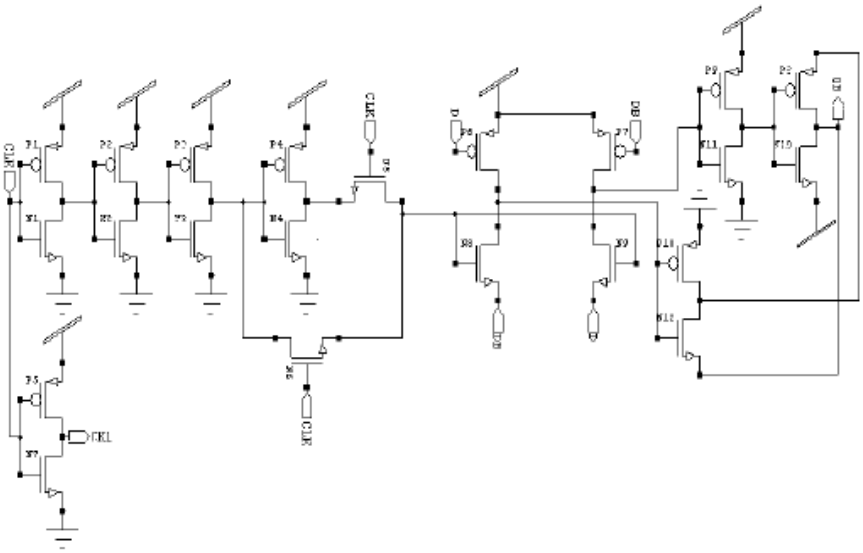

Fig.4: Schematic of Explicit pulsed proposed SAFF

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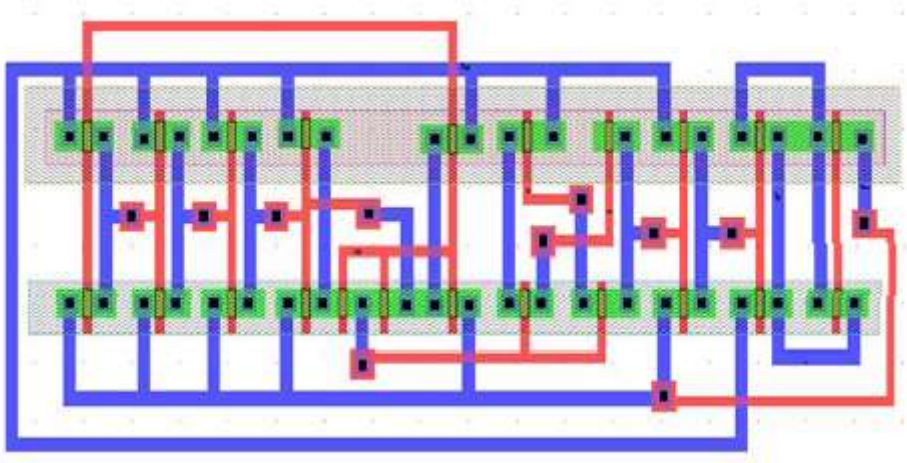

Fig.5: Explicit pulsed proposed SAFF layout

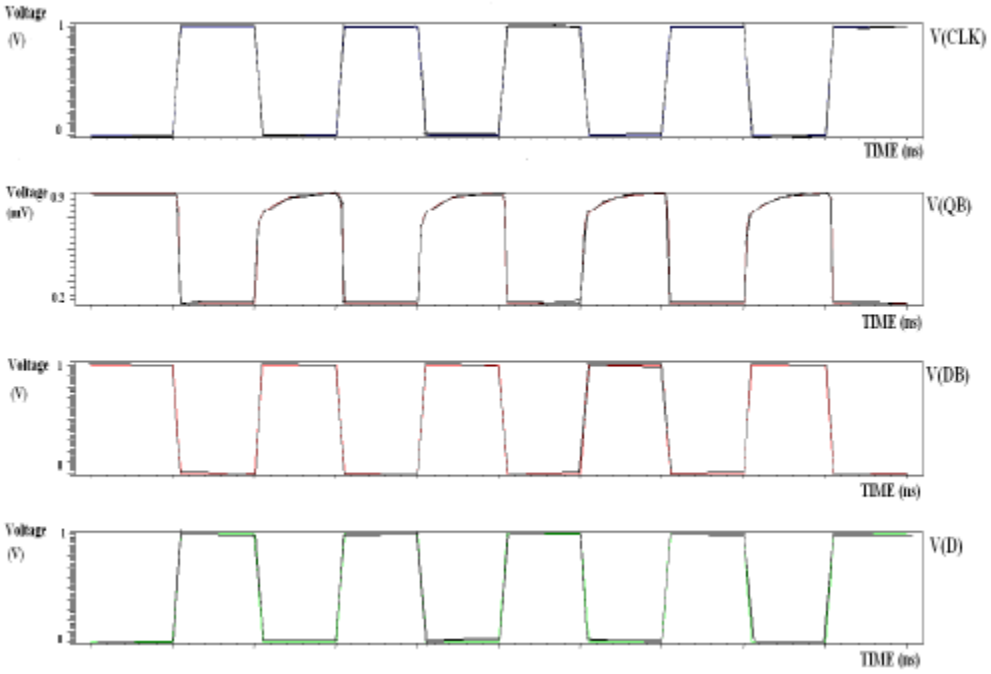

Fig.6: Waveforms of Explicit pulsed proposed SAFF

Explicit pulsed design of proposed SAFF is beneficial in that case when there are numerous neighboring SAFF's. Only one pulse generator, embedded on single chip, is sufficient to give power supply to entire chip.

III. SIMULATION AND COMPARISON

Simulation Environment:

All the circuits have been simulated using BSIM3v3 45 nm technology on Tanner EDA tool. To make the impartial testing environment, all the circuits have been simulated on the same input patterns. All experimental results for temperature, frequencies and supply voltages are carried out at VDD=1.25 V.

Pre-Layout Simulation of Explicit pulsed proposed SAFF (EP SAFF):

Pre-layout simulation graphs for explicit pulsed proposed SAFF are given below. Fig. 7 shows power consumption variation versus temperature. Fig.8-12 show delay variation, power consumption variation versus supply voltage, delay variation versus frequency, power consumption and delay variation versus output load capacitance respectively.

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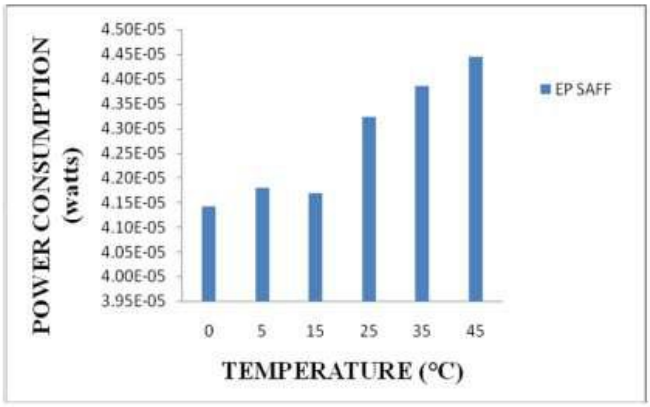

Fig.7: Power consumption variation over different operating ranges of temperature

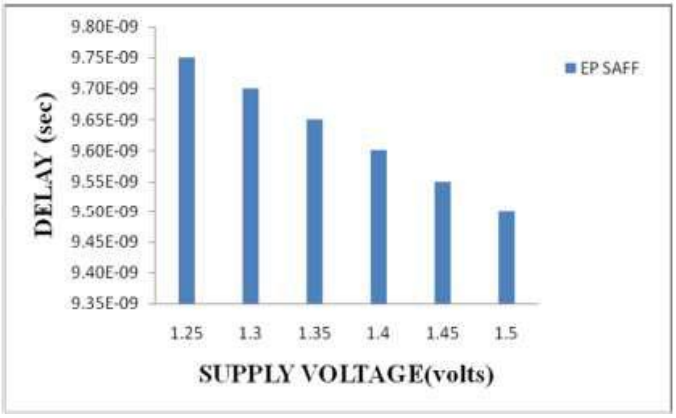

Fig.8: Delay variation over different operating ranges of supply voltage

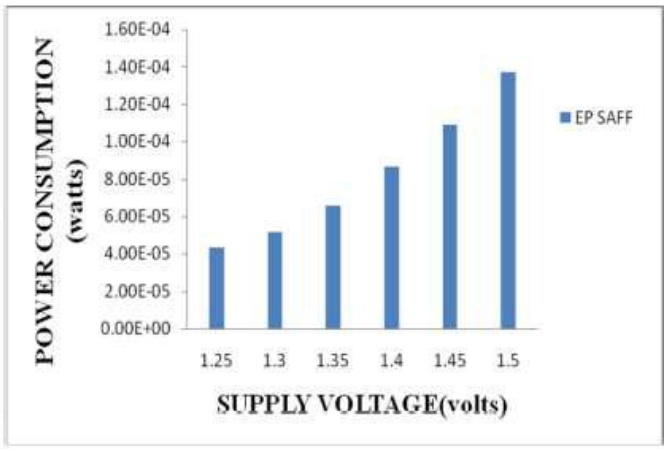

Fig.9: Power consumption variation over different operating ranges of supply voltage

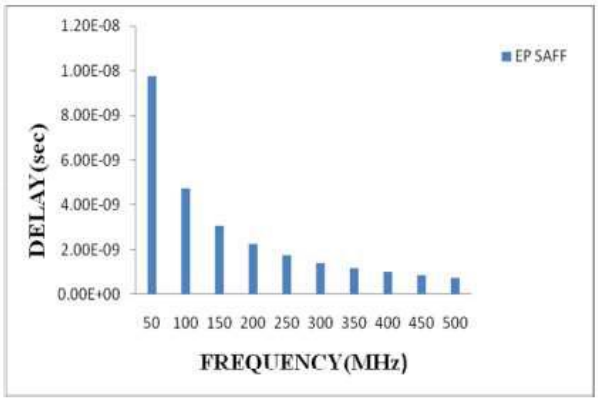

Fig.10: Delay variation over different operating ranges of frequency

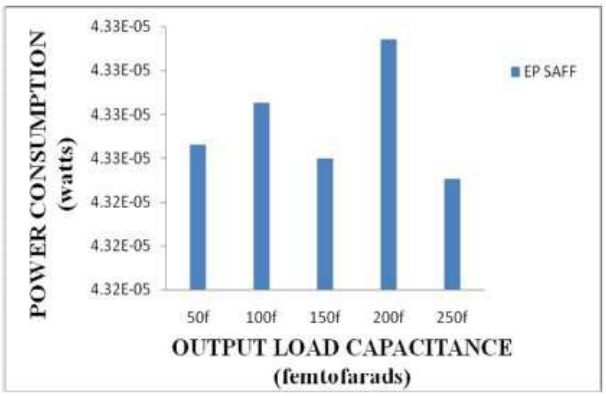

Fig.11: Power consumption variation over different values of output load capacitance

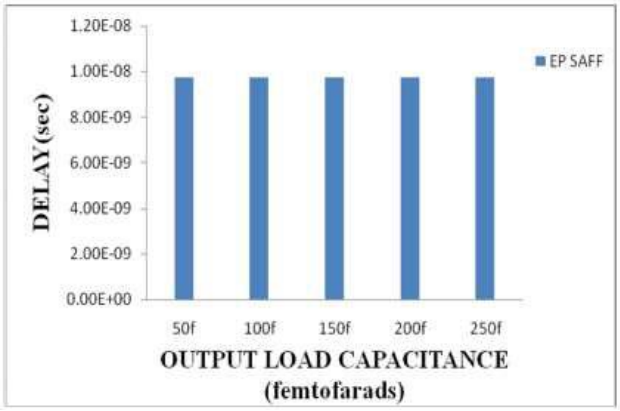

Fig.12: Delay variation over different values of output load capacitance

Post Layout Simulation of Explicit pulsed proposed SAFF:

Post-layout simulation results are shown with the help of following graphs.Fig.13 shows power consumption variation over different operating ranges of temperature.

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Power consumption is almost constant with temperature because of same order.Fig.14-15 shows power consumption and delay variation with supply voltage respectively.Fig.16 shows power consumption variation with frequency. Power consumption is continuously increasing with increase in frequency. Fig. 17 shows delay variation with respect to frequency.

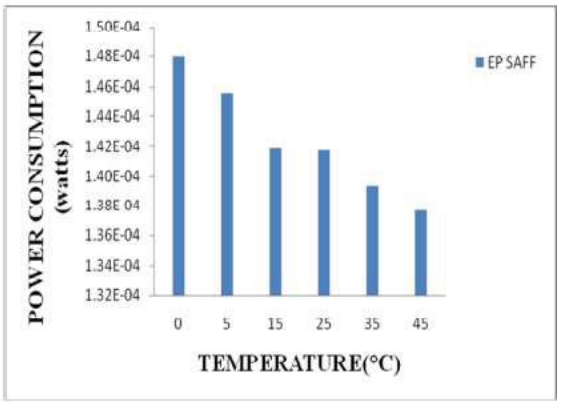

Fig.13: Power consumption variation over different operating ranges of temperature

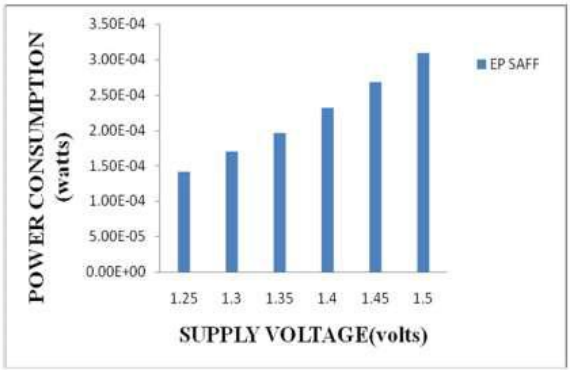

Fig.14: Power consumption variation over different operating ranges of supply voltage

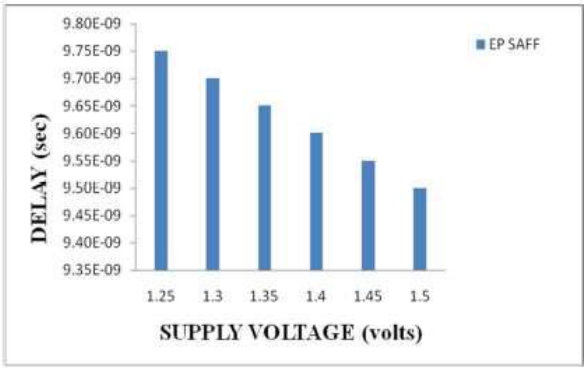

Fig.15: Delay variation over different operating ranges of supply voltage

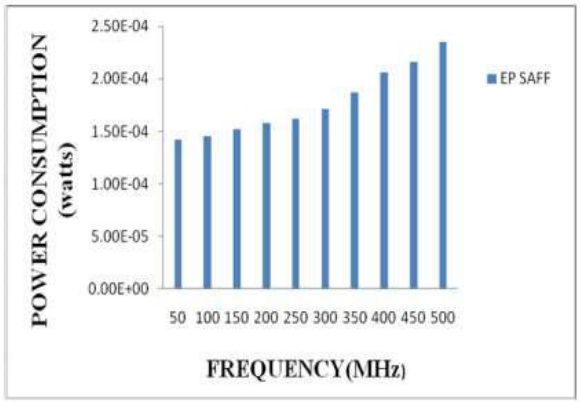

Fig.16: Power consumption variation over different operating ranges of frequency

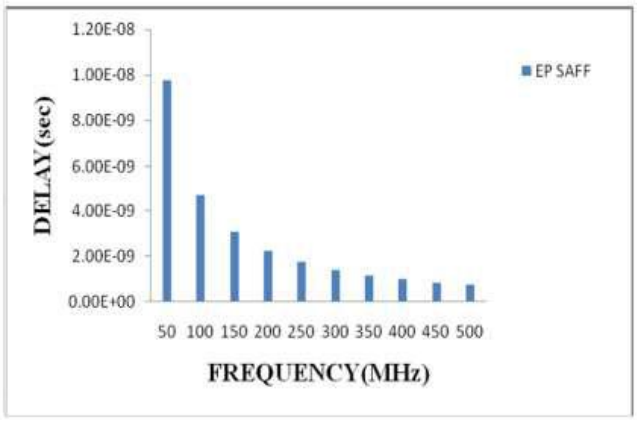

Fig.17: Delay variation over different operating ranges of frequency

At last, we designed explicit pulsed proposed SAFF and analyzed its simulation results.

IV. CONCLUSION

In this paper, we have proposed an explicit pulsed SAFF-GDI latch and compared it with implicit pulsed SAFF-GDI latch on the basis of its performance parameters i.e power consumption and delay over a wide range of temperature, supply voltages and frequencies. With the help of simulation results, it is proved that our proposed design of explicit pulsed SAFF is high performance and energy efficient over that of implicit pulsed SAFF-GDI latch.

ACKNOWLEDGMENT

The authors would like to thank Mody Institute of Technology & Science, Laxmangarh for supporting in carrying out this work.

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