https://dx.doi.org/10.22161/ijaers.4.4.17 *ISSN: 2349-6495(P) | 2456-1908(O)*

Low Power and Low Voltage Double Tail Dynamic Latch Comparator using 180nm Technology

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Abstract*—The requirement for highly integrated and programmable analog-to-digital converters (ADCs), area efficiency, and ultra-low-power and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to amplify speed and power efficiency. In this paper, analytical expressions are derived and an analysis on the delay of the dynamic comparators will be presented. From the analytical expressions, designers can obtain an instinct about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the analysis made, a new dynamic comparator is proposed, where the circuit of a conventional double tail comparator is modified for fast operation and low-power even in small supply voltages. By adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in an 180nm CMOS technology confirm the analysis results.*

***Keywords*— Double-tail comparator, dynamic clocked comparator, high-speed analog-to-digital converters (ADCs), low-power analog design.**

I. INTRODUCTION

ANALOG-TO-DIGITAL converters (ADCs) are being continuously driving towards their performance limits as technology scales down and system specifications become more challenging. Comparator is one of the basic fundamental building blocks in most analog-to-digital converters (ADCs). Many high speed ADCs, such as flash ADCs, require low power, maximum-speed comparators with compact chip area. High-speed comparators in ultra-deep sub-micrometer (UDSM) CMOS technologies tolerate low supply voltages especially when considering that the threshold voltages of the devices have not mount at the same rate as the supply voltages of the modern CMOS operation [1]. Hence, design of high-speed comparators is more challenging when the provided supply voltage is smaller. In other words, in a given technology, to achieve high speed, large numbers of transistors are required to compensate the reduction of supply voltage, which also means that more chip area and power is needed. Besides, low-supply-voltage operation results in limited common-mode input range, which is important for many high-speed ADC architectures, such as flash ADCs. Many techniques, such as techniques employing body-driven transistors [2], [3],current-mode design [4] , supply boosting methods [5],[6] and those using dual-oxide processes, which can handle higher supply voltages have been developed to undergo the low-voltage design challenges. Bootstrapping and boosting are two techniques based on raising the supply, reference, or clock voltage to mark input-range and switching problems. These techniques are effective, but they introduce reliability barriers especially in UDSM CMOS technologies. Despite the advantages, the body-driven transistor tolerate smaller trans-conductance (equal to g_{mb} of the transistor) compared to its gate-driven equivalent while particular fabrication process, such as deep n-well is needed to have both nMOS and pMOS transistors operate in the body-driven layout. Apart from technological modifications, developing new circuit structures which avoid stacking too many transistors between the supply voltages is preferable for low-voltage operation, especially if they do not expand the circuit complication. Body-driven technique embrace by Blalock [2], removes the threshold voltage necessity such that body-driven MOSFET operates as a depletion-type device. Based on this approach, in [3], a 1-bit quantizer for sub-1V $\sum\Delta$ modulator is proposed. In [7]–[9], additional circuit is added to the conventional dynamic comparator to enhance the speed of a comparator when provided with low supply voltages. The proposed comparator of [7] works down with a provided supply voltage of 0.5 V with a maximum provided clock frequency of 600 MHz and consumes 18 μW. Despite the advantages of this approach, the effect of component mismatch in the additional circuit on the performance of the comparator

https://dx.doi.org/10.22161/ijaers.4.4.17 *ISSN: 2349-6495(P) | 2456-1908(O)*

should be examined. The structure of double-tail dynamic comparator first proposed in [10] is based on designing a separate input and cross-coupled stage. This separation allows fast operation over a wide common-mode and supply voltage range [10]. In this paper, an inclusive analysis about the delay of dynamic comparators has been made for various architectures. Furthermore, based on the double-tail circuitry proposed in [10], a new dynamic comparator is presented, which does not need boosted voltage or stacking of too many transistors. Simply by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly minimized. This moderation also results in significant power savings when compared to the conventional dynamic comparator and double-tail comparator. The rest of this paper is categorized as follows. Section II explores the operation of the conventional clocked regenerative comparators and the pros and cons of each structure are discussed. Delay review is also presented and the analytical expressions for the delay of the comparators are obtained. The proposed comparator is presented in Section III. Section IV discusses the design issues. Simulation results are shown in Section V, followed by conclusions in Section VI.

II. CLOCKED REGENERATIVE COMPARATORS

The Clocked regenerative comparators have found vast applications in many high-speed ADCs since they can frame quick decisions due to the extreme positive feedback in the regenerative latch. Latterly, many comprehensive analyses have been presented, which explore the performance of these comparators from different aspects, such as offset [12], [13], and [14], noise [11], kick-back noise [16] and random decision errors [15]. In this section, a complete delay analysis is presented, the delay time of two common structures, i.e. Conventional dynamic double-tail comparator and conventional dynamic comparator are examined, based on which the proposed comparator will be presented.

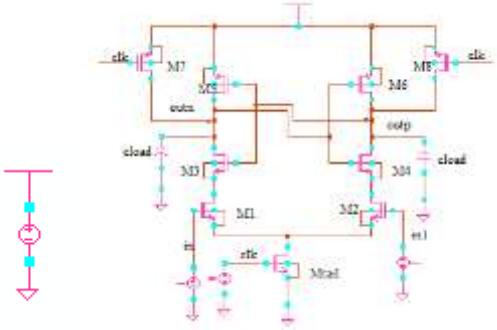

Fig.1: Schematic diagram of the conventional dynamic comparator

A. Conventional Dynamic Comparator

The schematic diagram of the conventional dynamic comparator generally used in A/D converters, with high input impedance, no static power consumption and rail-to-rail output swing, is shown in Fig.1 [1], [17]. A differential amplifier is consisting of pMOS and nMOS transistor (*M3, M4, M5, M6*) with combination of current mirror consisting of nMOS transistor (*M1, M2*), transistor *M7* and *M8* are used in the circuitry parallel to the differential amplifier. Two input voltages are used *INN, INP* provided to transistors *M1* and *M2* respectively. The operation of the comparator is as follows:-

During the reset phase i.e. when *CLK = 0* then the nMOS transistor *Mtail* is *OFF* , because when provided input logic level is low it turns off the nMOS, which reset pMOS transistors (*M7–M*8) pull both output nodes *Outn* and *Outp* to *VDD* to define a start state and to have a valid logical level during reset. In the comparison phase i.e. when *CLK = VDD*, pMOS transistors *M*7 and *M*8 are *OFF*, and *Mtail* is *ON*, because when provided input logic level is high it turns on the nMOS. Output voltages (*Outp, Outn*), which had been pre-charged to *VDD*, start to discharge with different discharging rates based on the corresponding input voltage (*INN/INP*). Assuming the case where *VINP > VINN*, *Outp* discharges faster than compare to *Outn*, hence when *Outp* (discharged by the nMOS transistor *M2* drain current), falls down to *VDD–|Vthp|* before the node *Outn* (discharged by transistor *M*1 drain current), the corresponding pMOS transistor (*M5*) will turn *ON* actuate the latch regeneration caused by back-to-back inverters (*M*3, *M*5 and *M4, M6*). Thus, *Outn* is pulled upto *VDD* and *Outp* discharges to ground. Case, if *VINP < VINN*, then the circuits works vice versa.

The delay of this comparator is comprised of two time delays, i.e. *t0* and t_{latch}. Where, the delay *t0* of the comparator represents the capacitive discharge of the load capacitance C_{load} till the first p-channel transistor i.e. either *M5* or *M6* turns *ON*. In case, the voltage at the node *INP* is greater than the voltage at node *INN (i.e., VINP > VINN)*, the drain current of the nMOS transistor *M2 (I2)* causes faster discharge of *Outp* node as compared to the *Outn* node, which is driven by transistor *M1* with smaller current. Hence, the discharge delay (*t*0) is given by

$$t_0 = C_{load}\frac{|V_{thp}|}{I_2} \cong 2C_{load}\frac{|V_{thp}|}{I_{tail}} \quad (1)$$

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In (1), since $I_2 = \frac{I_{tail}}{2} + \Delta I_{in} = \frac{I_{tail}}{2} + g_{m1,2}\Delta V_{in}$, for a small differential input (V_{in}), I_2 can be approx. to be persistent and is equal to the half of the tail current. Whereas, t_{latch}, is the latching delay of two cross-coupled inverters, it is assumed that a voltage swing of $\Delta V_{out} = \frac{V_{DD}}{2}$ has to be obtained from an initial output voltage difference V_0 at the falling output. Half of the supply voltage is considered to be the threshold voltage of the comparator following inverter or the SR latch. Hence, the latch delay time is given by,

$$t_{latch} = \frac{C_{load}}{g_{m,eff}} \ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) = \frac{C_{load}}{g_{m,eff}} \ln\left(\frac{V_{DD}/2}{\Delta V_0}\right) \quad (2)$$

Whereas, $g_{m,eff}$ is the effective trans-conductance of the back-to-back inverters. In fact, this delay determined, in a logarithmic way, at the beginning of the regeneration on the initial output voltage difference (i.e., when t=t_0). Based on (1), V_0 can be calculated from (3)

$$\Delta V_0 = \left|V_{outp}(t=t_0) - V_{outn}(t=t_0)\right|$$
$$= \left|V_{thp}\right| - \frac{I_2 t_0}{C_{load}} = \left|V_{thp}\right|\left(1 - \frac{I_2}{I_1}\right) \quad (3)$$

The current difference, $\Delta I_{in} = |I_1 - I_2|$ between the branches is much smaller than the current I_1 and I_2. Thus, I_1 can be approximated by $I_{tail}/2$ and (3) can be rewritten as

$$\Delta V_0 = \left|V_{thp}\right| \frac{\Delta I_{in}}{I_1} \approx 2\left|V_{thp}\right| \frac{\Delta I_{in}}{I_{tail}}$$
$$= 2\left|V_{thp}\right| \frac{\sqrt{\beta_{1,2} I_{tail}}}{I_{tail}} \Delta V_{in}$$
$$= 2\left|V_{thp}\right| \frac{\sqrt{\beta_{1,2}}}{I_{tail}} \Delta V_{in} \quad (4)$$

In the above equation, $\beta_{1,2}$ is the input transistor's current factor and I_{tail} is the function of input common-mode voltage (V_{cm}) and *VDD*. Substituting V_0 in latch delay expression and considering t_0, the equation for the delay of the conventional dynamic comparator is obtained as

$$t_{delay} = t_0 + t_{latch}$$
$$= C_{load} \frac{|V_{thp}|}{I_2} + \frac{C_{load}}{g_{m,eff}} . \ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right)$$
$$= 2C_{load} \frac{|V_{thp}|}{I_2} + \frac{C_{load}}{g_{m,eff}} . \ln\left(\frac{\Delta V_{DD}/2}{\Delta V_0}\right)$$
$$= 2C_{load} \frac{|V_{thp}|}{I_{tail}} + \frac{C_{load}}{g_{m,eff}} . \ln\left(\frac{V_{DD}}{4|V_{thp}|\Delta V_{in}} \sqrt{\frac{I_{tail}}{\beta_{1,2}}}\right) \quad (5)$$

Equation (5) elaborates the impact of various parameters. The overall delay is inversely proportional to the input difference voltage (V_{in}) and directly proportional to the comparator load capacitance C_{load}. Besides, the delay depends in-directly on the input common-mode voltage (V_{cm}). By reducing V_{cm}, the delay t_0 of the first phase increases because lower V_{cm} causes smaller bias current i.e. (I_{tail}). Whereas, (4) shows that a delayed discharge with smaller I_{tail} results in an increased initial voltage difference (V_0), reducing t_{latch}. Simulation output show that the effect of minimizing the V_{cm} on increasing of t_0 and reducing of t_{latch} will finally lead to an increase in the overall delay. In it has been shown that the input common-mode voltage is 70% of the supply voltage is optimal regarding speed and yield.

In principle, this design has the advantage of high no static power consumption, input impedance, rail-to-rail output swing, and good strength against noise and mismatch. Due to the factor that parasitic capacitances of input transistors do not instantly affect the switching speed of the nodes at the output, it is possible to design large input transistors to minimize the offset. Whereas, the disadvantage is the fact that due to several stacked transistors, a tolerably high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the conclusion, only transistors *M3* and *M4* of the latch contribute to the positive feedback until the voltage level of one output node has fall below a level small enough to turn "*ON*" transistors *M5* or *M6* to initiate complete regeneration. At a low supply voltage, this voltage drop only give a small gate-source voltage for transistors *M3* and *M4*, where the gate to source voltage of *M5* and *M6* is also very small, thus, the delay time of the latch becomes large due to lower trans-conductance. Another important drawback of this design is that there is only one current way, via tail transistor *Mtail*, which defines the current for the latch (the cross-coupled inverters) and for both the differential amplifier. While a small tail current is required to keep the differential pair in weak inversion interval and a better g_m/I ratio, a large tail current would be needed to enable fast regeneration in the latch. Besides, as far as *Mtail* conduct mostly in triode region, the tail current depends on the input common-mode voltage, which is not advantageous for regeneration.

B. Conventional Double-Tail Dynamic Comparator

A conventional double-tail comparator is shown in the below figure. This topography has less stacking and therefore it can operate at low supply voltages compared to the conventional dynamic comparator. The double tail allow both a large current in the latching stage and wider *Mtail2*, for fast latching unconventional of the input common-mode voltage (V_{cm}), and a small current in the input level (small Mtail1), for low offset .The operation of this comparator is as follows. During reset phase clock (*CLK = 0*,so transistor *Mtail1*, and *Mtail2* are OFF),transistors M3-M4 pre-charge

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the *fn* and *fp* nodes to *VDD*, which in turn causes transistors MR_1 and MR_2 to discharge the output nodes to ground. During decision-making phase i.e. when (*CLK* = *VDD*, then transistors *Mtail1* and *Mtail2* turn *ON*), transistors *M3-M4* turn *OFF* and voltages at nodes *fn* and *fp* start to drop with the rate defined by $IM_{tail1} / C_{fn(p)}$ and on top of this, an input-dependent differential voltage $V_{fn(p)}$ will build up.

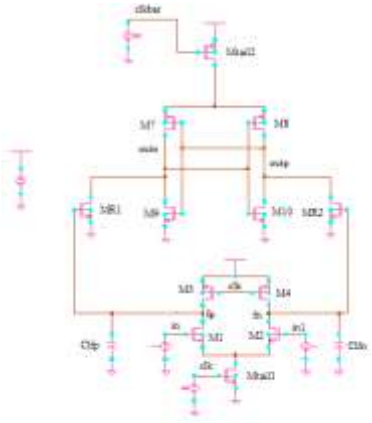

Fig.2: Schematic diagram of the conventional double-tail dynamic latch comparator

Same to the conventional dynamic comparator, the delay of this comparator comprises two main parts, t_0 and t_{latch}. The delay t_0 represents the capacitive charging of the load capacitance $C_{loadout}$ (at the latch stage output nodes, *Outn* and *Outp*) until the first n-channel transistor (*M9/M10*) turns *ON*, after which the latch regeneration starts, thus t_0 is obtained from

$$t_0 = \frac{V_{THN} C_{Loadout}}{I_{B1}} \approx 2\frac{V_{THN} C_{Loadout}}{I_{tail2}} \quad (6)$$

Where I_{B1} is the drain current of the transistor *M9* (assuming *VINP* >*VINN*) and is equal to approx. of the half of the tail current (I_{tail2}). After the first n-channel transistor of the latch turns on (for the instance, M_9), the corresponding output (e.g., *Outn*) will be discharged to the ground, leading front p-channel transistor to turn on, charging another output (*Outp*) to the supply voltage (*VDD*). The regeneration time (t_{latch}) is reached according to equation (2). For the initial output voltage difference at time t_0, V_0 we have

$$\Delta V_0 = \left|V_{outp}(t=t_0) - V_{outn}(t=t_0)\right| = V_{THN} - \frac{I_{B2} t_0}{C_{loadout}}$$

$$= V_{THN}\left(1 - \frac{I_{B2}}{I_{B1}}\right) \quad (7)$$

Where I_{B2} and I_{B1} are the currents of the left latch and right side branches of the second stage, respectively

Considering I_{latch} = |IB1 - IB2| = *gm R*1, 2Vfn/fp, (7) can be rewritten as

$$\Delta V_0 = V_{THN}\frac{\Delta I_{latch}}{I_{B1}} \approx 2V_{THN}\frac{\Delta I_{latch}}{I_{tail2}} = 2V_{THN}\frac{g_m R_{1,2}}{I_{tail2}}\Delta V f_n / f_p \quad (8)$$

Where $gmR_{1,2}$ is the trans-conductance of the intermediate stage transistors (MR_1 and MR_2) and *Vfn/fp* is the difference in voltage at the first stage outputs (*fn* and *fp*) at time *t0*. Thus, it can be observed that two main parameters which influence the initial output differential voltage *(V_0)* and therefore the latch regeneration time is the trans-conductance of the intermediate stage transistors *($gmR_{1,2}$)* and the voltage difference of the first stage outputs (*fn* and *fp*) at time *t0*. In fact, intermediate stage transistors amplify the voltage difference of *Vfn/fp* causing the latch to be disparity. The differential voltage at nodes *fn/fp* *($V_{fn}/_{fp}$)* at time *t0* can be achieved from

$$\Delta V_{fn/fp} = \left|V_{fn}(t=t0) - V_{fp}(t=t0)\right|$$

$$= t_0 \cdot \frac{I_{N1} - I_{N2}}{C_{Load,fn(p)}}$$

$$= t_0 \cdot \frac{g_{m1,2}\Delta V_{in}}{C_{Load,fn(p)}} \quad (9)$$

In the above equation, I_{N1} and I_{N2} refer to the discharging currents of input transistors (*M1* and *M2*), which are dependent on the input difference voltage (i.e., *IN* = *gm1*, *2Vin*). Substituting (9) in (8), *V0* will be

$$\Delta V_0 = 2V_{Thn}\frac{g_m R_{1,2}}{I_{tail2}}\Delta V_{fn/fp}$$

$$= \left(\frac{2V_{THN}}{I_{tail2}}\right)^2 \frac{C_{loadout}}{C_{load,fn(p)}} g_{mR1,2} g_{m1,2} \Delta V_{in} \quad (10)$$

This equation shows that *V0* depends strongly on the trans-conductance of input and intermediate stage transistors, input voltage difference (*Vin*), the capacitive ratio of $C_{Loadout}$ to $C_{Load,fn(p)}$ and latch tail current.

Some important notes can be concluded.

1) The difference in voltage at the first stage outputs (*Vfn/fp*) at time *t0* has a great effect on latch initial differential output voltage (*V0*) and consequently on the latch delay. Therefore, increasing it would greatly reduce the delay of the comparator.
2) In this comparator, both intermediate stage and transistors will be finally cut-off, (since *fn* and *fp* nodes both discharge to the ground), hence they do not play any important role in improving the effective trans-conductance of the latch. Besides, during reset phase, these nodes have to be charged from ground to *VDD*, which means power utilized.

https://dx.doi.org/10.22161/ijaers.4.4.17 *ISSN: 2349-6495(P) | 2456-1908(O)*

III. PROPOSED DOUBLE-TAIL DYNAMIC COMPARATOR

Fig.3 indicates the schematic diagram of the proposed dynamic double-tail comparator. Because of the better performance of double-tail architecture in low-voltage applications, the proposed comparator design is based on the double-tail structure. The main objective of the proposed comparator is to increase *V*fn/fp in order to increase the latch regeneration speed. For this the, two control transistors (*Mc1* and *Mc2*) have been added to the first stage of proposed idea in parallel to *M3/M4* transistors but in a cross-coupled manner.

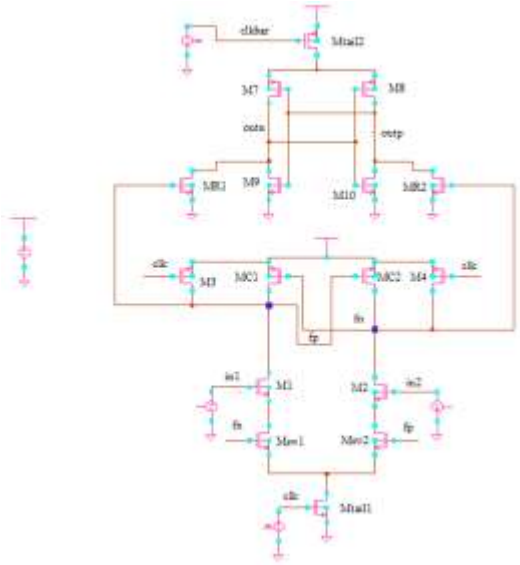

Fig.3: Schematic diagram of the proposed dynamic comparator

A. Operation of the Proposed Comparator

The operation of proposed comparator is as follows. During reset phase i.e., when (CLK = 0) transistor *Mtail1* and *Mtail2* are OFF (avoiding static power), transistor *M3* and *M4* pulls both nodes *fn* and *fp* to *VDD*, hence transistor *Mc1* and *Mc2* are in cut off region. Intermediate stage transistors i.e., *MR1* and *MR2*, reset both latch outputs to ground. During decision-making phase i.e., when (CLK = *VDD*) transistor *Mtail1*, and *Mtail2* are ON, transistors *M3* and *M4* turn OFF. Further, at the beginning of this phase, the control transistors are OFF (and transistor *fn* and *fp* are charged to *VDD*). Thus, transistor *fn* and *fp* start to drop with different rates according to the provided input voltages. Suppose *VINP* > *VINN*, then *fn* drops faster than *fp*, (because *M2* provides more current than *M1*). Since *fn* continues to fall, the corresponding pMOS control transistor (*Mc1* in this case) starts to turn ON, pulling other node *fp* back to the *VDD*; so another control transistor (*Mc*2) remains OFF, allowing *fn* to be discharged completely. Whereas, unlike conventional double-tail dynamic comparator, in which *Vfn/fp* is just a function of input voltage difference and input transistor trans-conductance , in the proposed architecture as soon as the comparator detects that for instance *fn* node discharges faster, a pMOS transistor (*Mc1*) turns on, pulling the node *fp* back to the *VDD*. Hence, by the time passing, the difference between *fn* and *fp (Vfn/fp*) increases in an exponential manner, leading to the reduction of latch regeneration time. In spite the effectiveness of the proposed architecture, one of the points which should be considered is that in this circuit, when one control transistor (e.g., *Mc1*) turns ON, input and tail transistor (e.g., *Mc1*, *M1*, and *Mtail1*) draw current from *VDD* to the ground , resulting in static power consumption. To overcome the issue of static power consumption, two nMOS switches [*Msw1* and *Msw2*] are used below the input transistors.

At the beginning of the decision making phase, due to the fact that both nodes *fn* and *fp* have been pre-charged to *VDD* (during the reset phase), both switches i.e., *Msw1* and *Msw2* are closed and *fn* and *fp* start to drop with different discharging rates. As soon as the comparator finds that one of the node *fn/fp* is discharging faster, control transistors will act to increase their voltage difference. Suppose that node *fp* is pulling up to the *VDD* and node *fn* should be discharged completely, hence the switch in the charging path of *fp* will be opened (in order to prevent any current drawn from *VDD*) but the other switch connected to node *fn* will be closed to allow the complete discharge of *fn node*. That is the operation of the control transistors with the switches follows the operation of the latch.

B. Delay Analysis

In order to theoretically signify how the delay is reduced, delay equations are derived for this structure the proposed dynamic comparator maximizes the speed of the double-tail comparator by affecting two important factors., first, it rise the initial output voltage difference (*V0*) at the beginning of the regeneration ($t = t0$); and second, it enhances the effective trans-conductance (g_{meff}) of the latch.

1) *Effect of Enhancing V*0*:* Time after which latch regeneration starts is *t0*,we can say *t0* is considered to be the time it takes (while both latch outputs are rising with different rates) until the first nMOS transistor of the cascaded inverters turns on, so that it will pull down one of the outputs and regeneration will commence.

https://dx.doi.org/10.22161/ijaers.4.4.17 *ISSN: 2349-6495(P) | 2456-1908(O)*

$$\Delta V0 = V_{Thn}\frac{\Delta I_{latch}}{I_{B1}}$$
$$\approx 2V_{Thn}\frac{\Delta I_{latch}}{I_{tail2}}$$
$$= 2V_{Thn}\frac{g_m R_{1,2}}{I_{tail2}}\Delta V_{fn/fp} \quad (11)$$

To find *Vfn/fp* at $t = t0$, it is important to notice that the combination of the control transistors (*Mc1* and *Mc2*) with two serial switches (*Msw1*, *Msw2*) follow the operation of a cascaded inverter pair; *Vfn/fp* is calculated by

$$V_{fn/fp} = V_{fn(p)0}\exp((A_v - 1)t/\tau) \quad (12)$$

Where in the equation, $\frac{\tau}{A_v - 1} \cong \frac{C_{L,fn(p)}}{G_{m,eff1}}$ and $\Delta V_{fn(p)0}$ is the initial fn/fp difference node voltage corresponding pMOS control transistor in turned ON. Hence, $\Delta V_{fn(p)0}$ can be obtained from-

$$\Delta V_{fn(p)0} = 2|V_{Thp}|\frac{g_{m1,2}\Delta V_{in}}{I_{tail1}} \quad (13)$$

Substituting (12) in (13), *V*0 will be

$$\Delta V = 2V_{Thn}\frac{g_{m1,2}}{I_{tail2}}\Delta V_{fn/fp}$$
$$= 4V_{Thn}|V_{Thp}|\frac{g_{mR1,2}}{I_{tail2}}\frac{g_{m1,2}\Delta V_{in}}{I_{tail1}}\exp\left(\frac{G_{m,eff1}.t_0}{C_{L,fn(p)}}\right) \quad (14)$$

Comparing (14) with (10), it is observed that *V*0 has been increased remarkably (in an exponential manner) in compare with the conventional dynamic comparator.

2) Effect of Enhancing Latch Effective Trans-conductance: In conventional double-tail comparator, both the nodes fn and fp finally discharge's completely. In the proposed comparator, one of the first stage output (fn/fp) nodes will charge up to the *VDD* at the beginning of the decision making phase, and will turn ON one of the intermediate stage transistors, thus the effective trans-conductance of the latch is maximized. That is positive feedback is strengthened. Hence, t_{latch} will be

$$t_{latch} = \frac{C_{Lout}}{g_{m,eff} + g_{mR1,2}}.\ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right)$$
$$= \frac{C_{Lout}}{g_{m,eff} + g_{mR1,2}}.\ln\left(\frac{VDD/2}{\Delta V_0}\right) \quad (15)$$

Finally,including both the effects-

$$t_{delay} = t_0 + t_{latch}$$
$$= 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff} + g_{mR1,2}}.\ln\left(\frac{VDD/2}{\Delta V_0}\right)$$
$$= 2\frac{V_{Thn}C_{Lout}}{I_{tail2}} + \frac{C_{Lout}}{g_{m,eff} + g_{mR1,2}}.\ln\left(\frac{VDD/2}{4V_{Thn}|V_{Thp}|\frac{g_{mR1,2}}{I_{tail2}}\frac{g_{m1,2}\Delta V_{in}}{I_{tail1}}\exp\left(\frac{G_{m,eff1}.t_0}{C_{L,fn(p)}}\right)}\right) \quad (16)$$

By comparing the expressions it can be seen that the proposed comparator takes gain of an inner positive feedback in double-tail operation, which strengthen the latch regeneration. This speed improvement is even clearer in lower supply voltages. This is due to the fact that for larger values of V_{Th}/VDD, the trans-conductance of the transistors minimizes, thus the existence of an inner positive feedback in the structure of the first stage will lead to the comparator's improved performance.

3) Reducing the Energy per Comparison: In the modified proposed comparator, the energy per conversion is reduced as well delay parameter is also improved. As discussed earlier, in conventional double-tail topology, both nodes fn and fp discharge to the ground during the period of decision making and each time during the reset phase they should be pulled up back to the *VDD*. However, in proposed comparator, only one of the nodes (fn/fp) has to be charged during the reset phase. This is because during the previous decision making phase, based on the status of control transistors, one of the nodes had not been discharged and thus less power is required.

IV. DESIGN CONSIDERATIONS

While determining the size of tail transistors i.e., (*Mtail1* and *Mtail2*), it is necessary to ensure that the time it takes that one of the control transistors turns on must be smaller than *t0*.This condition can be achieved by properly designing the first and second stage tail currents.

$$t_{on,Mc1(2)} < t_0 \prec \frac{|V_{Thp}|.C_{L,fn(p)}}{I_{n1,2}} < \frac{V_{Thn}C_{Lout}}{I_{B1}}$$
$$\prec \frac{|V_{Thp}|.C_{L,fn(p)}}{\frac{I_{tail1}}{2}} < \frac{V_{Thn}C_{Lout}}{\frac{I_{tail2}}{2}} \quad (17)$$

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In designing the nMOS switches, the drain-source voltage of these switches must be considered since it might limit the voltage headroom, restricting the advantage of being used in low-voltage applications. In order to reduce this effect, low-on-resistance nMOS switches are required. In other words, large transistors can be used. Since the parasitic capacitances of these switches do not affect the parasitic capacitances of the nodes fn/*fp*, it is possible to select the size of the nMOS switch transistors in a way that both low-voltage and low-power operations are maintained.

A. Mismatch Analysis

In principle, the situation where input differential voltage (*Vin*) is very small where *fn* and *fp* have approximately similar discharging rates except this, the effect of current factor mismatch and threshold voltage mismatch of controlling transistors is almost negligible in most cases. The differential input signal is already amplified to large amplitude compared to the mismatches by the time that the controlling transistor (*M*c1 or *M*C2) turns ON. In other words, offset due to the controlling transistor mismatches is divided by the gain from the input to the output. However, in case of small *Vin*, when nodes fn and *fp* follow each other tightly, the mismatch of the controlling transistors might influence the result of the comparison. Hence, the following brief analyzes the effect of current and threshold factor mismatches of controlling transistors on the total input-referred offset voltage.

1) *Effect of Threshold Voltage Mismatch of transistor M*C1, *M*C2, *i.e., VThC1, 2*: Due to the threshold voltage mismatch the differential current can be obtained from

$$i_{diff} = g_{mc1,2}\Delta V_{Thc1,2} \qquad (18)$$

Where, *g*mc1, 2 is the trans-conductance of the controlling transistors. So, the input-referred offset voltage due to the *Mc1, 2* threshold voltage mismatch is obtained as follows:

$$\Delta V_{eq,due\Delta V_{Thc1,2}} = \frac{g_{mc1,2}\Delta V_{Thc1,2}}{g_{m1,2}}$$

$$= \frac{\mu_p W_{C1,2} V_{ODC1,2}}{\mu_n W_{1,2} V_{OD1,2}} \Delta V_{Thc1,2} \qquad (19)$$

2)*Effect of Current-Factor Mismatch M*C1, *M*C2, *i.e.*$\Delta\beta$C1,2: In order to find the input-referred offset due to the

current factor mismatch of *M*C1,2, $\Delta\beta$C1,2 is modeled as a channel width mismatch ΔW, i.e., $\Delta\beta/\beta = \Delta W/W$.

$$i_{diff} = \frac{1}{2}\mu_p c_{ox}\frac{\Delta W}{L}\left(V_{gsc1,2} - V_{thc1,2}\right)^2 \qquad (20)$$

B. Kickback Noise

Principally in latched comparators, on the regeneration nodes the large voltage variations are coupled, through the parasitic capacitances of the transistors, to the input of the comparator. Since the circuit introduce it does not have zero output impedance, the input voltage is disturbed, due to which there may be degradation in accuracy of the converter. This disturbance is usually called "kickback noise." However it improves the double-tail topology in terms of energy per comparison and thus operation speed, the kickback noise is increased in comparison to conventional double-tail structure.

V. SIMULATION RESULTS

To compare the proposed comparator with the conventional and double-tail dynamic comparators, all three circuits have been simulated in a 0.18-μm CMOS technology with power supply *VDD* = 1.2 V. The comparators were optimized and the transistor dimensions were scaled.

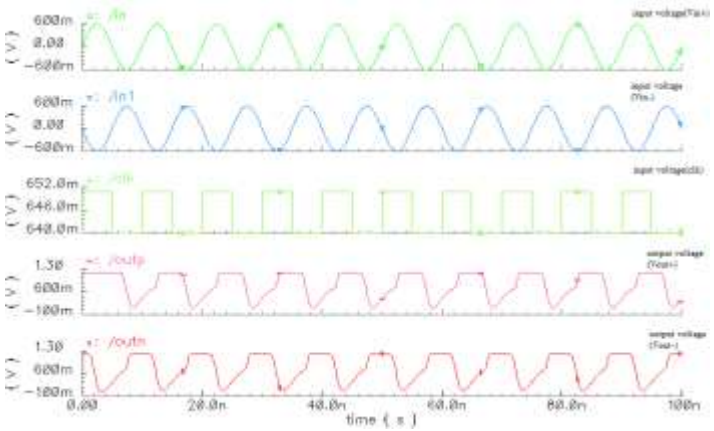

Fig.4: Transient analysis of Conventional Dynamic Latch Comparator

https://dx.doi.org/10.22161/ijaers.4.4.17 *ISSN: 2349-6495(P) | 2456-1908(O)*

Table.1: result of conventional dynamic latch comparator

Design parameters	**Comparator Value**
Technology	180nm
Supply voltage	1.2 V
Slew rate+	265.498 M V/ns
Slew rate-	706.615M V/ns
Rise time	4ns
Fall time	2ns
Hold time	3ns
Delay	5ns
Power dissipation	93.49µw

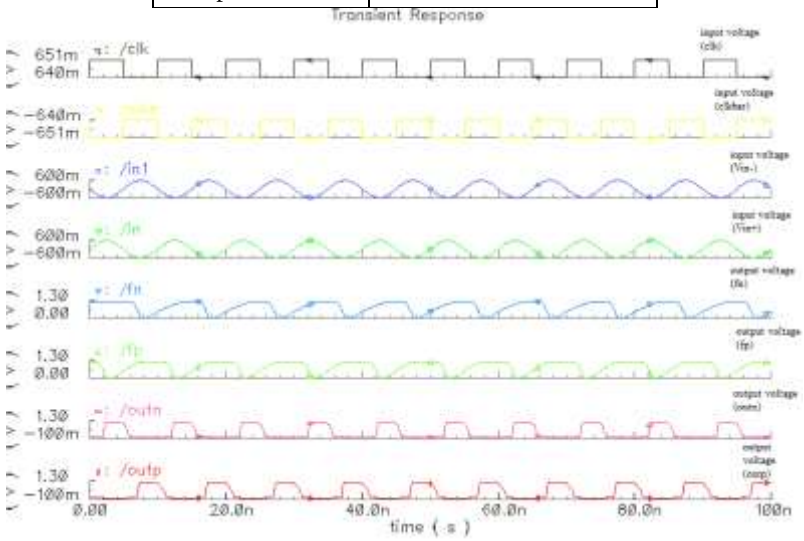

Fig.5 Transient analysis of Conventional Double Tail Dynamic Latch Comparator

Table.II: result of conventional double tail dynamic latch comparator

Design parameters	**Comparator Value**
Technology	180nm
Supply voltage	1.2 V
Slew rate+	2.84G/ns
Slew rate-	1G/ns
Rise time	1.6ns
Fall time	2ns
Hold time	4ns
Delay	4ns
Power dissipation	25.25uw

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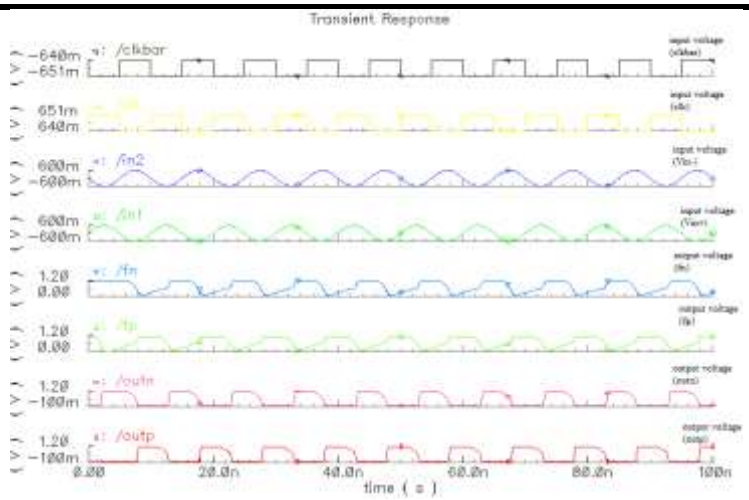

Fig.6: Transient analysis of proposed Comparator

Table.III.:Result of proposed comparator

Design parameters	**Comparator Value**
Technology	180nm
Supply voltage	1.2 V
Slew rate+	3.02006G
Slew rate-	577.531M
Rise time	0.5ns
Fall time	1ns
Hold time	3ns
Delay	2ns
Power dissipation	22.4456µw

VI. CONCLUSION

In this paper, a comprehensive delay analysis for clocked dynamic comparators is presented and expressions were derived. Two common structures conventional double-tail dynamic comparator and of conventional dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation of the circuit results in 0.18-μm CMOS technology confirmed that the energy per conversion and delay of the proposed comparator is reduced to a great extent in comparison with the double-tail comparator and conventional dynamic comparator.

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