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Study of Electron Transport in Fullerene (C_{60}) Quantum Confined Channel Layer Based Field Effect Transistor

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Abstract— *In this work, we modelled a simple n-channel Si Metal-Quantum confined layer-Semiconductor Field Effect Transistor (MQSFET), which resembles exactly as the conventional Si Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) where SiO_2 dielectric layer is replaced with a wide band gap C_{60} quantum confined layer of thickness 3nm and gold (Ψ=5.1eV) as metal contact. The capacitance and voltage characteristics at different temperatures from 100 K to 500 K and energy band gap are studied using Multi-dielectric Energy Band Diagram Program (MEBDP) simulation software, performed current-voltage transistor characteristics and analyzed the mobility of the charge carrier in the MQS sandwiched device structure using the Caughey-Thomas high saturation mobility model and the Lombardi surface mobility model. In these studies, we inferred a very low threshold voltage, when the donor concentration in the p-Si substrate is tuned between 1E16 to 1E17 cm^{-3} and a saturated flow of nanoamperes range of charge carrier at a low gate potential is even possible.*

Keywords— C_{60}, quantum confined layer, Metal-Quantum Confined Layer-Semiconductor Field Effect Transistor (MQSFET), Multi-dielectric Energy Band Diagram Program (MEBDP), Capacitance-Voltage characteristics, Current-Voltage characteristics, Mobility modelling.

I. INTRODUCTION

Gordon Moore prophesied that transistor built on a single die of the Si chip doubles every eighteen months [1, 2]. With respect to the Moore's law, the gate length of the MOSFET will eventually shrink to 5 nm by 2020 [3]. As the transistor feature size keeps decreasing, the enhancement in the VLSI MOSFET device models is essential so that the exact behavior of deep sub-micron and nanometer scaled MOSFETs can be defined with accuracy. When we keep miniaturizing the MOSFET, there is a reduction in charge transport (also known as carrier mobility) [4, 5]. The reduction in charge transport is the prime cause of drain current degradation. This reduces the switching speed of the device [6]. Hence, carrier mobility on the surface inversion has been of great interest in MOSFET can be studied using various mathematical modeling [7, 8]. In this work, we use Caughey-Thomas mobility (CTM) model and Lombardi surface mobility (LSM) model to study the charge mobility performance of the proposed C_{60} quantum confined layer, a thin film of 3 nm thickness as gate dielectric layer.

CTM model helps to demonstrate a high field velocity scattering to an existing mobility models such as constant input mobility [9]. Above the ambient thermal energy, the charge carriers can gain energy, with an added input of the applied field. Thus, this gained energy can be able to transfer from the applied field to the lattice. This is due to the optical phonon emission. Field dependent mobility makes a problem which is already highly non-linear. It is hence important to use the continuation study extension to obtain convergence in the high field limit [10].

This model helps us to determine the electron ($\mu_{n,ct}$) and hole ($\mu_{p,ct}$) mobility by the following equations:

$$\mu_{n,ct} = \frac{\mu_{in,n}}{\left(1+\left(\frac{\mu_{in,n} F_n}{v_{sat,n}}\right)^{\alpha_n}\right)^{1/\alpha_n}} \quad (1)$$

$$\alpha_n = \alpha_{0,n}\left(\frac{T}{T_{ref}}\right)^{\beta_{1,n}} \quad (2)$$

$$v_{sat,n} = v_{0,n}\left(\frac{T}{T_{ref}}\right)^{\beta_{2,n}} \quad (3)$$

$$\mu_{p,ct} = \frac{\mu_{in,p}}{\left(1+\left(\frac{\mu_{in,p} F_p}{v_{sat,p}}\right)^{\alpha_p}\right)^{1/\alpha_p}} \quad (4)$$

$$\alpha_p = \alpha_{0,p}\left(\frac{T}{T_{ref}}\right)^{\beta_{1,p}} \quad (5)$$

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$$\upsilon_{sat,p} = \upsilon_{0,p}\left(\frac{T}{T_{ref}}\right)^{\beta_{2,p}} \quad (6)$$

where T: the lattice temperature (K),
F_n and F_p: the driving forces for electrons & holes
$F_n=E_{\parallel,n}$: component of the electric field parallel to the electron current
$F_p=E_{\parallel,p}$: component of the electric field parallel to the hole current
$\mu_{in,n}$ and $\mu_{in,p}$: the electron and hole input mobility.
$\upsilon_{0,n}$ and $\upsilon_{0,p}$: the saturation velocities for electrons and holes (m/s)

All the other parameters used in the model are the material properties of Si [11-14, 30-31] (Refer Appendix).

The Lombardi surface mobility model is used for understanding the electron mobility in a simplified MOSFET (Metal Oxide Semiconductor Field Effect Transistor) [15]. We can compare the current density profile and total current flowing into the terminal with the constant mobility model. Especially in the thin inversion layer under the gate in MOSFETs, two factors have an important effect on the carrier mobility. They are the surface roughness and the surface acoustic phonons. This model adds interesting resultant effects with the surface scattering to the already existing Matthiessen's rule-based modeling [16]. The electron mobility ($\mu_{n,lo}$) and hole mobility ($\mu_{p,lo}$) are calculated by the following equations:

$$\frac{1}{\mu_{n,lo}} = \frac{1}{\mu_{in,n}} + \frac{1}{\mu_{ac,n}} + \frac{1}{\mu_{sr,n}} \quad (7)$$

$$\mu_{ac,n} = \frac{\mu_{1,n}}{\left(\frac{E_{1,n}}{E_{ref}}\right)} + \frac{\mu_{2,n}\left(\frac{N}{N_{ref}}\right)^{\beta_n}}{\left(\frac{E_{\perp,n}}{E_{ref}}\right)^{1/3}\left(\frac{T}{T_{ref}}\right)} \quad (8)$$

$$\mu_{sr,n} = \frac{\delta_n}{E_{\perp,n}^2} \quad (9)$$

$$\frac{1}{\mu_{p.lo}} = \frac{1}{\mu_{in,p}} + \frac{1}{\mu_{ac,p}} + \frac{1}{\mu_{sr,p}} \quad (10)$$

$$\mu_{ac,p} = \frac{\mu_{1,p}}{\left(\frac{E_{1,p}}{E_{ref}}\right)} + \frac{\mu_{2,p}\left(\frac{N}{N_{ref}}\right)^{\beta_p}}{\left(\frac{E_{\perp,p}}{E_{ref}}\right)^{1/3}\left(\frac{T}{T_{ref}}\right)} \quad (11)$$

$$\mu_{sr,p} = \frac{\delta_p}{E_{\perp,p}^2} \quad (12)$$

$$N = N_a^- + N_d^+ \quad (13)$$

where T: the lattice temperature (K),
N_a^- and N_d^+: the ionized acceptor and donor concentration,
$E\perp_{,n}$ & $E\perp_{,p}$: the component of the electric field perpendicular to the electron and hole current,
$\mu_{in,n}$ and $\mu_{in,p}$: the electron and hole input mobility,
δ_n and δ_p: the delta coefficients for electrons and holes (V/s).

All other parameters in the model are the material properties of silicon. (Refer Appendix).

We choose buckminsterfullerene (C_{60}), because of its excellent properties. It includes: wide bandgap, high dielectric properties, withstand high temperatures, possess great current density, fast switching speed and less on-resistance. It is also an active element in n-channel field effect transistor, because of its very high electron mobility. [18, 19].

II. DEVICE THEORY AND MODELLING

As portrayed in figure 1, C_{60} Quantum structure embedded thin film layer of thickness 3nm is deposited on the p-Si substrate [20-23]. The source and drain are the n-type Si. Au is used as gate metal. We characterized this MQS structure as a capacitor and a FET structure. Hence we analyzed the capacitance-voltage (CV) characteristics, current-voltage (IV) characteristics and charge transport behavior in different mobility models.

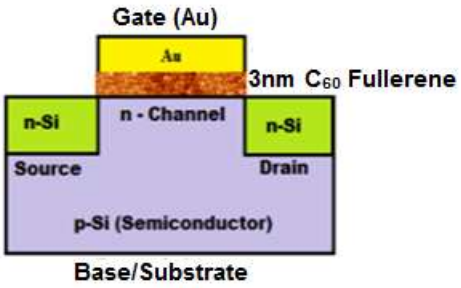

Fig.1: Proposed structure of MQSFET using 3nm C60 quantum confined layer

A. Caughey-Thomas Mobility Model

In this model, we swept the drain to source voltage from 0 to 1 V, at no applied field (Vgs=0V). Sweeping the drain voltage creates an important electric field at the left side of the gate at the junction between the n-doped and p-doped regions. In order to ensure convergence of the linear model, a solver continuation parameter is used to rise up the electron and the hole driving forces (Fn and Fp) as the drain voltage is swept. Table 1 shows the CTM model parameters for Si [26,27].

Table.1: CTM model parameters for Si

Description	Value
Electron alpha coefficient	1.11
Hole alpha coefficient	1.21
Electron saturation velocity	1E7[cm/s]
Hole saturation velocity	8.37E6[cm/s]
Electron alpha exponent	0.66

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Hole alpha exponent	0.17
Electron velocity saturation exponent	-0.87
Hole velocity saturation exponent	-0.52
Reference temperature	300[K]

B. Lombardi Surface Mobility Model

In this model, when the gate voltage of 1V is applied, the drain voltage is swept from 0V to 1V. We can observe an important perpendicular electric field to the flow of charges underneath the gate contact. In order to ensure convergence of the nonlinear model, a solver continuation parameter is used to rise up the electron and hole perpendicular to the field ($E_{\perp, n}$ and $E_{\perp, p}$), as the drain voltage is swept [24, 25]. Table 2 shows the LSM model parameters for Si [26-29].

Table.2: LSM model parameters for Si

Description	Value
Electron delta coefficient	5.82E14[V/s]
Hole delta coefficient	2.05E14[V/s]
Electron mobility reference	4.75E7[cm^2/(V*s)]
Hole mobility reference	9.93E7[cm^2/(V*s)]
Electron mobility reference	1.74E5[cm^2/(V*s)]
Hole mobility reference	8.84E5[cm^2/(V*s)]
Electron alpha coefficient	0.125
Hole alpha coefficient	0.0317
Reference temperature	1[K]
Electric field reference	1[V/cm]
Doping concentration reference	1[1/cm^3]

C. Other Parameters Used

The CTM model and the LSM model has the following parameters for the quantum confined layer C_{60}, as listed in Table 3.

Table.3: Description of C_{60} confined layer

Description	Value
Terminal name	3
Terminal type	Voltage
Voltage	Vgs
C_{60} relative permittivity	4.5
C_{60} layer thickness	tq = 3 [nm]
Au Metal work function	5.1 [V]

Table 4 shows the materials energy gap and dielectric constant values which are used in the modelling. The fullerene C_{60} acts as a gate channel, an active element in this MQSFET. C_{60} possess a band dap of 1.9eV and a dielectric constant (κ) of 4.5.

Table.4: Energy-gap (Eg) and dielectric constant (κ) of various materials

	Si	SiO_2	C_{60}
Band gap 'Eg' (eV)	1.12	9	1.9
Dielectric constant 'κ'	11.8	3.9	4.5

III. RESULTS AND DISCUSSIONS

Initially, we performed simulation for the Au/C_{60}/p-Si MQS structure using Multi-dielectric Energy Band Diagram Program (MEBDP) to study the energy band diagram of the proposed device, capacitance-voltage characteristics and CV at various temperatures. The flat band condition of the Au/C_{60}/p-Si MQS structure obtained at V_{fb} = -0.28V.

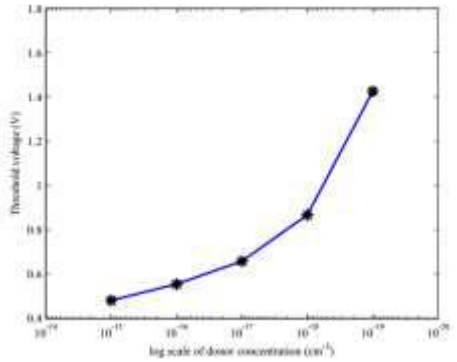

Fig.2: Threshold voltages at various log scale of donor concentrations.

Using MEBDP simulation software, we simulated the model. We inferred that the threshold voltage of this device can be tuned to our desirable value, as we keep decreasing the donor concentration of the p-Si substrate. As shown in figure 2, as the donor concentration of the p-Si substrate keeps increases, the threshold voltage of the device also increases.

The stack capacitance is calculated by sweeping the voltage from -5 to +5 V, at various temperatures 100 K to 500 K. The CV characteristics at various temperatures are shown in figure 3. From the CV characteristics, we study the accumulation, depletion and inversion occurrence in the device. As there is increase in temperature, the stack capacitance in the accumulation mode keeps increases. In the depletion region, there is a decrease in stack capacitance as the temperature increase and in the saturation region, there is a gradual increase in stack capacitance but lesser than the device capacitance, as the

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temperature increases. The device can work efficiently even at higher temperatures around 500K.

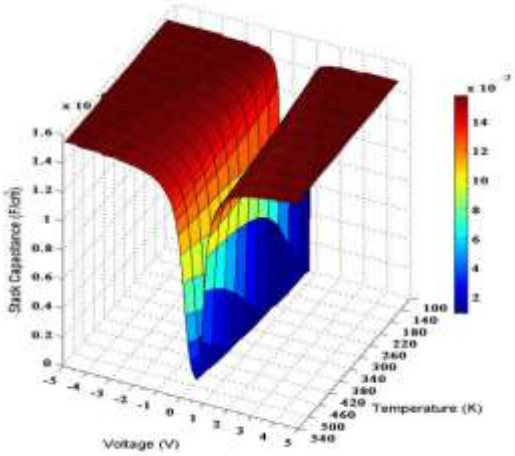

Fig.3: Stack capacitance Vs Voltage (CV) characteristics of the Au/C_{60}/p-Si MQS Capacitor at various temperatures.

Figure 4 shows the drain current versus gate voltage, for a fixed drain voltage of 10mV simulated for the C_{60} quantum confined nanolayer based MQSFET. From this plot, we found out that the threshold voltage (V_{th}) is approximately 0.8V. For a minimum drain voltage, the threshold voltage is little higher. For higher drain voltages, the threshold voltage will reduce below 0.8V. The switching of the device will be faster for higher drain voltages.

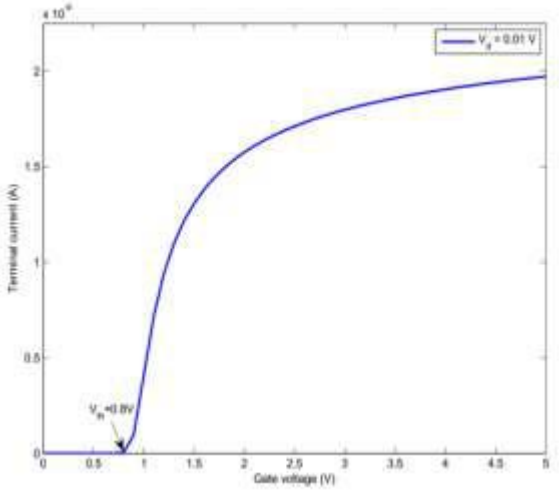

Fig.4: Drain current versus gate voltage at Vd = 0.01V of Au/C_{60}/p-Si MQSFET device.

Also for the quantum confined C_{60} nanolayer MQSFET, the drain current and drain voltage characteristics simulated and the characteristics plot for various gate voltages at Vg ranges from 1 to 4V shown in figure 5. It is very clear from the plot that, a linear region is seen at the low voltages, a nonlinear region at the intermediate voltages and saturation region at higher voltages. It is observed that a small current flow, when the gate voltage is very small and a maximum current flow saturated at the positive and greater gate voltages.

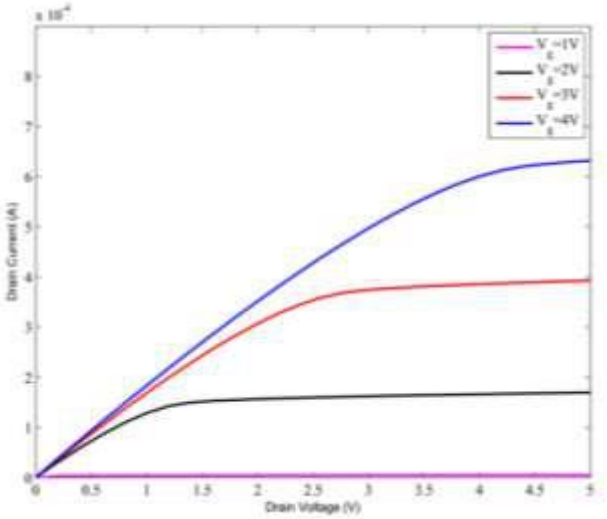

Fig.5: Drain current (I_d) vs drain voltage (V_d) characteristics of the Au/C_{60}/p-Si MQSFET device.

A. **Caughey-Thomas mobility model:**

Figure 6 shows the comparison of the terminal current for the constant mobility and Caughey-Thomas mobility of Au/C_{60}/p-Si MQSFET device. The effect of the CTM on the solution is well seen. The comparison of the constant mobility (the driving forces are multiplied by 1E-6) and the CTM (Fn and Fp multiplied by 1) models shows a more pronounced saturation effect for this model. The current is lower and level off more rapidly due to the fact that the mobility decreases when the electric field is high.

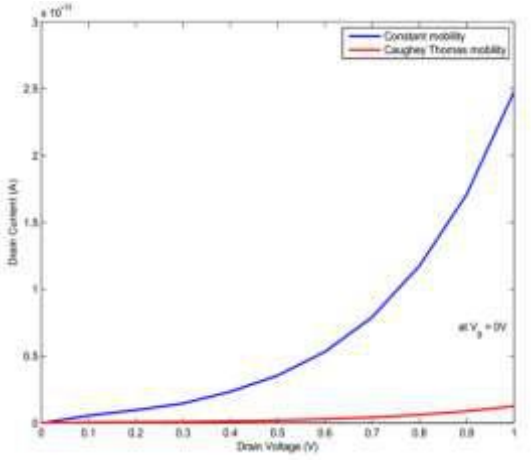

Fig.6: Comparison of the terminal current for the constant mobility and Caughey-Thomas mobility of Au/C_{60}/p-Si MQSFET device.

B. **Lombardi surface mobility model:**

The effect of the Lombardi surface mobility model of the Au/C_{60}/p-Si MQSFET device is shown in figure 7, which

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explains the comparison of the constant mobility (the perpendicular fields are multiplied by 1E-6) and the Lombardi surface mobility (E⊥,n and E⊥,p multiplied by 1) models shows a more pronounced saturation effect for the Lombardi surface mobility model than for the constant mobility model (without field dependent parameters).

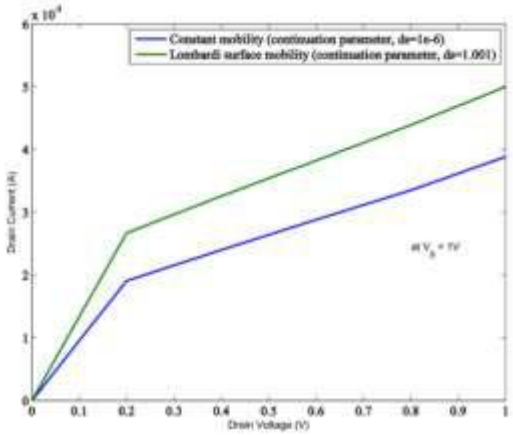

Fig.7: Plot of terminal current for the constant mobility and surface mobility cases of Au/C_{60}/p-Si MQSFET device. The current is inhibited when the surface mobility is active.

IV. CONCLUSIONS

Through the Caughey-Thomas mobility model, we studied that in C_{60} MQSFET, the current is lower and level off more rapidly due to the fact that the mobility decreases when the electric field is high. And the study from the Lombardi surface mobility model of C_{60} MQS FET explains that as a consequence of the inversion layer generated by the applied potential on the gate contact and due to the presence of C_{60} quantum layer bonded with the surface of the semiconductor Si, the electron mobility is slightly smaller in the vicinity of the C_{60} gate junction. Hence, C_{60} quantum confined layer can be able to work well as a gate dielectric channel and behave well as a better replacement for Si channel, for a low power and can withstand a high temperature upto 500K in future device applications.

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CONFLICT OF INTERESTS

The authors declare no conflict of interest.

AUTHOR CONTRIBUTIONS

Cyril R. A. John Chelliah - performed the simulation experiments, analyzed the data and wrote the article; Barbara Szymanik – contribution in teaching simulation using COMSOL; Rajesh Swaminathan - leading the research project, contributed ideas and suggestions.

SUPPLEMENTARY MATERIALS

Nanohub, Multidielectric Energy Band Diagram Program, COMSOL multiphysics.

APPENDIX

Material properties of Silicon	Value	Unit
Relative permittivity	11.7	1
Electron lifetime, SRH	10[us]	S
Hole lifetime, SRH	10[us]	S
Band gap	1.12[V]	V
Electron affinity	4.05[V]	V
Effective density of states, valence band	(T/300[K])^(3/2)*1.04E19[1/cm^3]	1/m^3
Effective density of states, conduction band	(T/300[K])^(3/2)*2.8E19[1/cm^3]	1/m^3
Hole mobility	500[cm^2/(V*s)]	m^2/(V*s)
Electron delta coefficient	5.82E14[V/s]	V/s
Hole delta coefficient	2.05E14[V/s]	V/s
Electron mobility reference	4.75E7[cm^2/(V*s)]	m^2/(V*s)
Hole mobility reference	9.93E7[cm^2/(V*s)]	m^2/(V*s)
Electron mobility reference	1.74E5[cm^2/(V*s)]	m^2/(V*s)
Hole mobility reference	8.84E5[cm^2/(V*s)]	m^2/(V*s)
Electron alpha coefficient	0.125	1
Hole alpha coefficient	0.0317	1
Reference temperature	1[K]	K

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Electric field reference	1[V/cm]	V/m
Doping concentration reference	1[1/cm^3]	1/m^3

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