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# Ultra High MULTI CLOCK FREQUENCY BAUD RATE 128 Bit Multichannel PRBS CODEC ASIC I.P Core Design for High speed wireless internet Wi-Fi Routers, MODEM's, NIC's

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***Abstract—*** *The main aim is for HDL Design and Implementation of 128 Bit Multichannel PRBS CODEC for High Speed wireless internet computing products like Wi-Fi Routers, MODEM's. this is very suit for very high speed internet computing products / applications of Big Parallel Network Data MODEM Interface based Computing Servers/Stations. This design consists of PRBS Encoder and Decoder Design of Different Channel Frequencies in terms of different PRBS Patterns Sequences – $2e^{7}$-1,$2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1, $2e^{48}$-1, $2e^{52}$-1, $2e^{64}$-1,$2e^{128}$-1 by tapping through different feedback elements. Tapping of PRBS Done as per C.C.I.T.T – I.T.U O.150,O.151,O.152,O.153 Standards . these pattern sequences are encoded and decoded through different PRBS channel type selector/de-selector and outputs are generated through serial and parallel form of different PRBS Patterns. Programming design description done by Verilog HDL/VHDL and Design Synthesis & Implementation done through Xilinx ISE Software and Debugging done by Advanced FPGA Development Boards/Kits. Design Verification done through highly proficient Test Bench/Stimulus Design Module Codes.*

***Keywords— HDL – Hardware Description Language , MODEM – Modulator Demodulator, CODEC – Coding Decoding, Wi-Fi – Wireless internet Fidelity, I.T.U – International Telecom Unit, C.C.I.T.T – Consulting Committee for International Telegraph and Telephone , PRBS – Pseudo Random Binary Sequence ,FPGA – Field Programmable Gate Array.***

## I. INTRODUCTION

In Advanced Modern Hi-tech Data Communication & Network Engineering world , Parallel Network Data Processing and controlling, Computing plays vital role in many electronic Data communication Computing and network engineering & IT products. Due to this I Designed Multichannel PRBS CODEC for transmission and reception of data processing through parallel computing of different channel baud-rate data speed of different channel frequencies. This is an 128 bit PRBS CODEC – generates multiple carrier waves modulates and demodulates with orginal base band data input signal of different channel frequency spectrum – simply spreading de-spreading the data. This codec is mainly suit for multiple baud rate frequency speed MODEM's, NIC's , Wi-FI routers. This is an heart of these products for computing data through big networking stations /servers. This is an high speed application product.

A. Basically MODEM "A modem (*modulator-demodulator*) is a device that modulates an analog carrier signal to encode digital information, and also demodulates such a carrier signal to decode the transmitted information. So it is Data Conversion Equipment". The MODEM encode and decode the carrier signal using Pseudo random Binary Sequence(PRBS) Pattern Codes of Different Pattern sequences $2e^{7}$-1,$2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1, $2e^{48}$-1, $2e^{52}$-1, $2e^{64}$-1,$2e^{128}$-1 ,and generation of ultra high speed frequencies. The goal is to produce a signal that can be transmitted easily and decoded to reproduce the original digital data. Modems are generally classified by the amount of data they can send in a given unit of time, usually expressed in terms of bits per second (bit/s, or bps), bytes/frames/super frames /very long word super frames/super very long word frames/packets of data rate. These signals can be

transmitted over telephone lines and demodulated by another modem at the receiver side to recover the digital data.

B. Modem, short for modulator-demodulator is an electronic device that converts a computer's digital signals into specific frequencies to travel over telephone or cable television lines. At the destination, the receiving modem demodulates the frequencies back into digital data. Computers use modems to communicate with one another over a network.

C. The wireless PRBS MODEM basically Designed for Encrypt and Decrypt Digital Data packets through wireless bus communication channel protocols of different broadband frequency spectrum for multiuser communication, the Wireless PRBS MODEM consists of Multichannel Encoder and Decoder and Wireless Channel Register Bus. This Wireless PRBS MODEM Support Data Speed In terms of Mega ,Giga, Tera, Peta, Exa, Zetta, Yotta, Xona, Weka, Vendica Bits Per second through Data Channel Bus.

D. The Wireless PRBS MODEM Chip Supports all 3G,4G,5G,6G wireless Computing applications.

E. At the source, modulation techniques are used to convert digital data (0's and 1's) into analog form for transmission across the channel. At the destination, the received analog signal is converted to digital data via demodulation. This is a simplified explanation of how a modem works, and there are other issues that require attention; such as channel impairments, encryption, error detection/correction, data compression, modulation, handshake negotiation, and echo cancellation.

## II. BASIC MODEM ARCHITECTURES

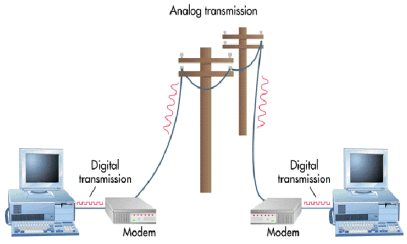


*Fig.1:Telephone MODEM Architecture*

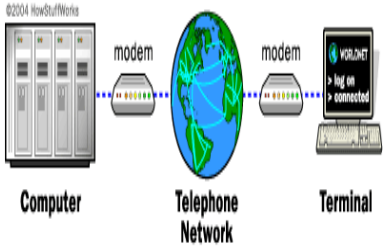


*Fig.2: Internet MODEM Architecture*

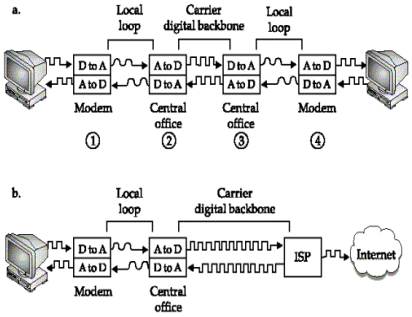


*Fig.3: PC to PC MODEM /CODEC*

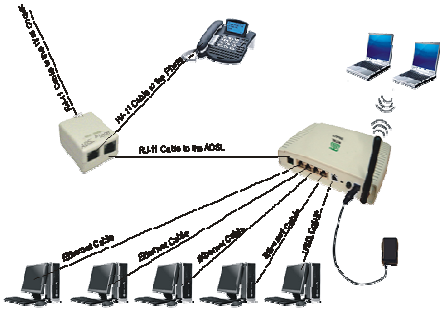

*Fig.4: Telephone-PC MODEM Architecture*

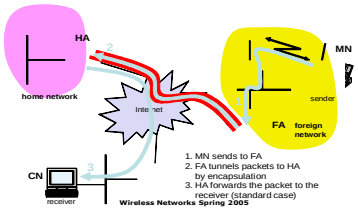


*Fig.5: Internet-PC MODEM Architecture*

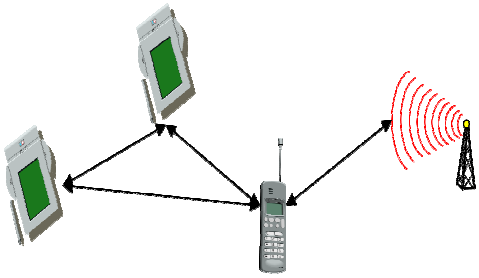

*Fig.6: Mobile-Mobile Service Architecture*

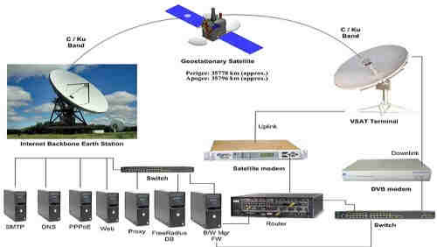

*Fig.7: Fixed Wireless Architecture*

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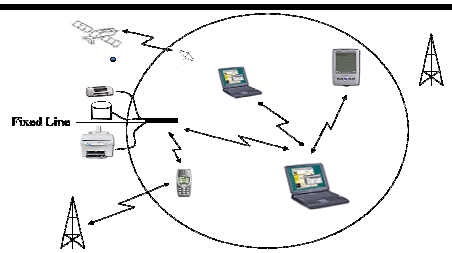



*Fig.8: Mobile Wireless Architecture*

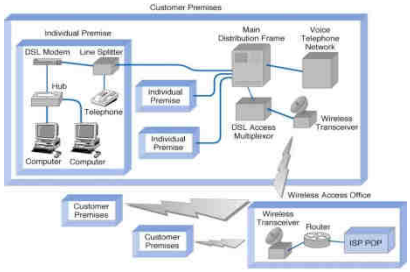



*Fig.9: Architecture Of Bluetooth wireless System*

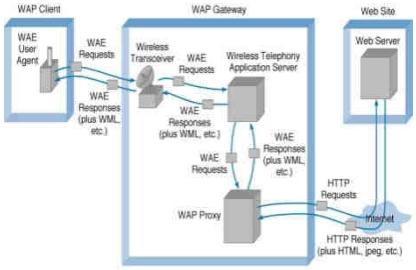



*Fig.10: Architecture of WAP Gateway*

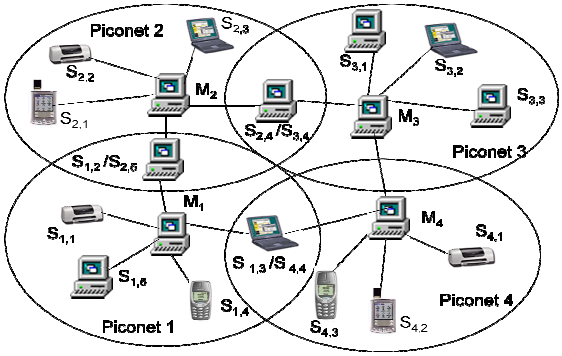



*Fig.11: Internet Network Architecture*

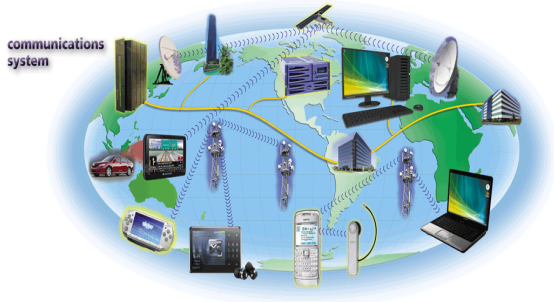
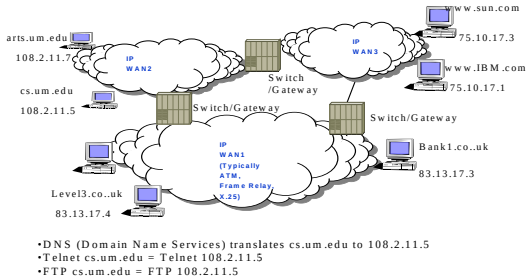



*Fig.12: Wireless WEB Architecture*




•DNS (Domain Name Services) translates cs.um.edu to 108.2.11.5
•Telnet cs.um.edu = Telnet 108.2.11.5
•FTP cs.um.edu = FTP 108.2.11.5

*Fig.13: WAP MODEM Architecture*

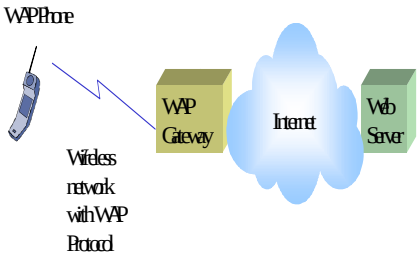



*Fig.14: Wireless Network VAP Gateway*

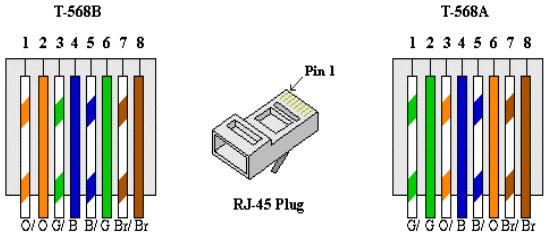



*Fig.15: RJ45 Communication Architecture*

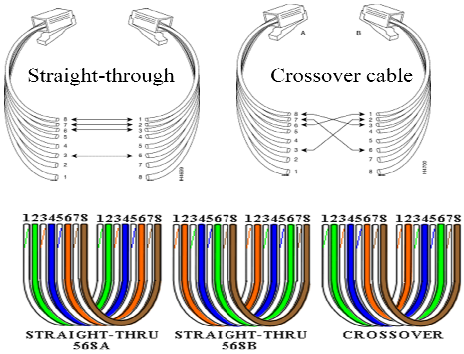



*Fig.16: Cross Over Communication Architecture*

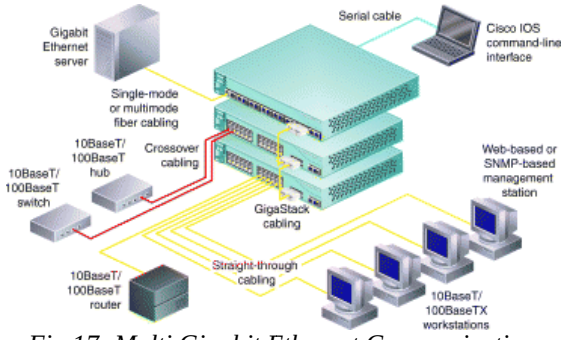



*Fig.17: Multi Gigabit Ethernet Communication Architecture*

2(A). Architecture Description: The Diagrams Above represents different Hi-tech MODEM Communication Architectures based on the Priority Levels and Data Communication Capacity, these are Basic Telephone wire

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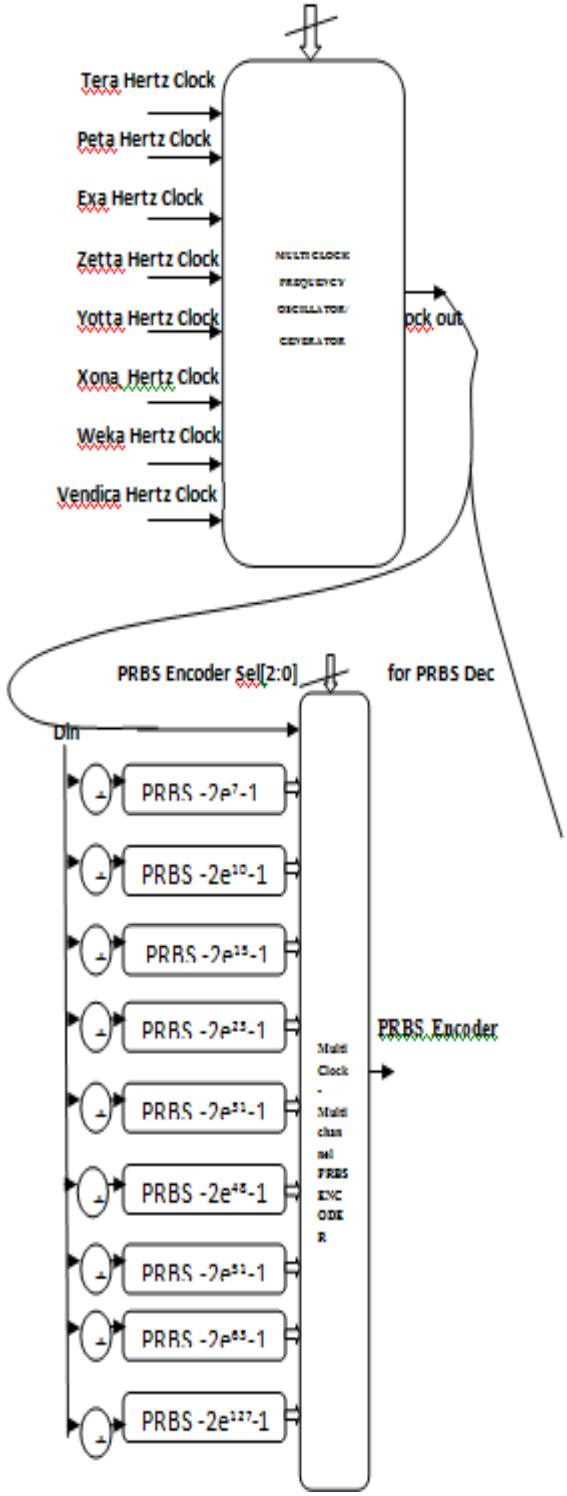
and wireless MODEM, Internet MODEM, PC-PC, Telephone-to-PC MODEM, Mobile to Mobile, Consumer Mobile MODEM, MODEM Server, Bluetooth, Internet,WAP, Wireless Web Data Network, Fixed, Mobile wireless , WAP MODEM, Giga bit Ethernet MODEM , Server Computing Station Architectures. These above are widely used for LAN , MAN,WAN Systems, Cloud Internet, Cluster, Parallel Distributed Network Computing Architectures. These are mainly used for parallel communication for number of multiple users and multiple applications for sharing large data processing and computing with out any data loss of Large Broad Frequency Band Spectrum of large wider frequency Bandwidth. Compared to above modems, I designed new top class generation Hi-tech Smart Wireless Computing PRBS MODEM Architecture of Different PRBS Carrier Frequency Patterns-$2e^{7}$-1,$2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1, $2e^{48}$-1, $2e^{52}$-1, $2e^{64}$-1,$2e^{128}$-1 PRBS Tapped Sequences for large multi user parallel communication and data computing. I'm Implemented the Wireless PRBS CODEC through HDL Design(Verilog and VHDL) , Data Transfer rate in terms of tera,peta ,exa,zetta,Yotta,xona,weka,Vendica Baud rate(Bits per Second). The wireless PRBS CODEC Consists of Different Cross Bar Router Switches for reducing the data traffic loss of large wide bandwidth. This is simply parallel distributed computing technique at a time data processing and computing done on number of multiple users. The speed of data is more than the internet modem because it is purely synchronized with tera,peta, exa,zetta,Yotta,xona,weka,Vendica clock frequencies.

## III. Ultra High MULTI CLOCK FREQUENCY BAUD RATE MULTICHANNEL WIRELESS PRBS MODEM/CODEC DESIGN ARCHITECTURE OF DIFFERENT PRBS PATTERN SEQUENCES



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**PRBS Decryption Architecture**

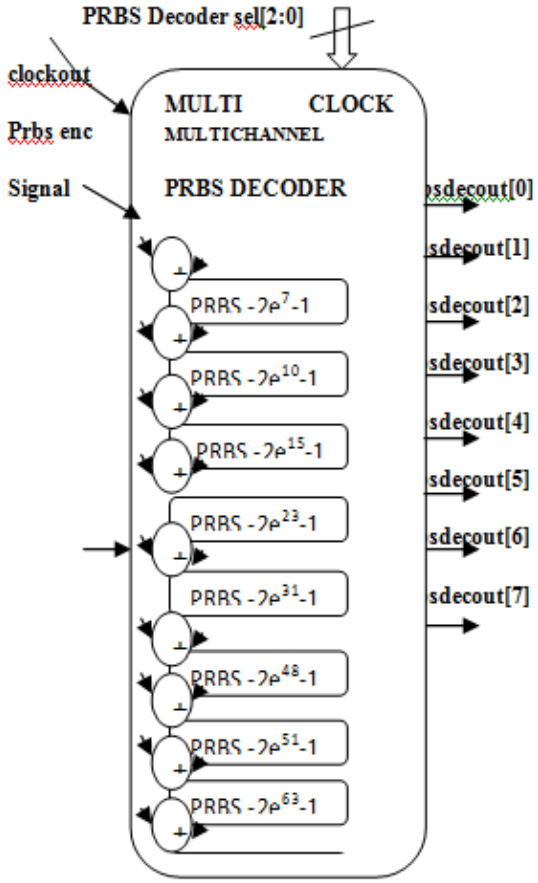
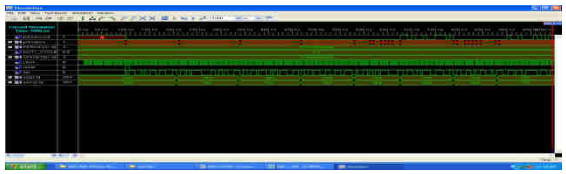


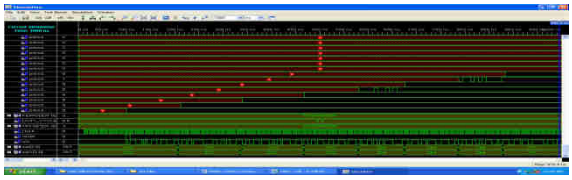

*Fig.18: Multichannel Wireless PRBS MODEM Architecture*

## IV. SIMULATION WAVE FORM RESULTS

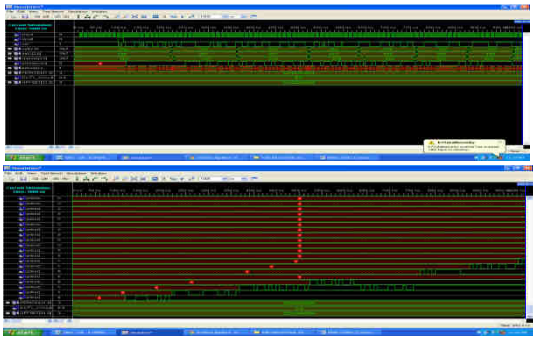
### A. PRBS ENCODER

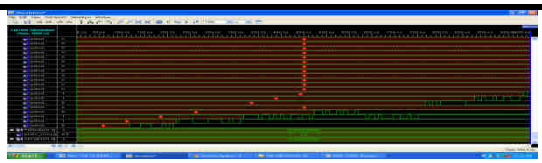


B. PRBS DECODER

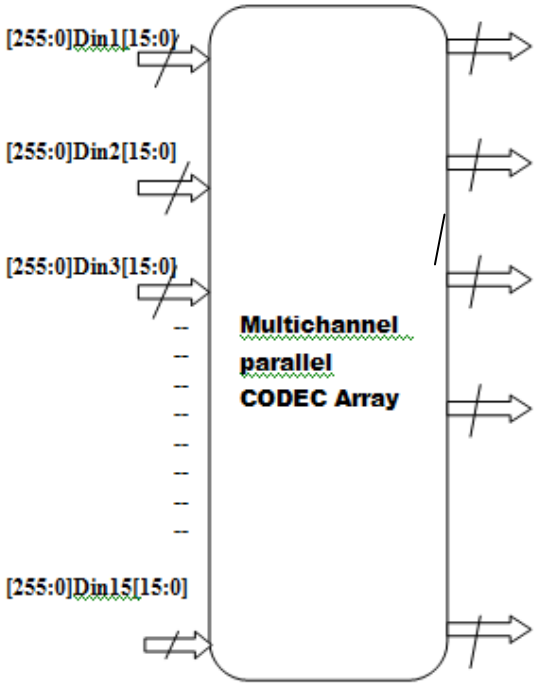


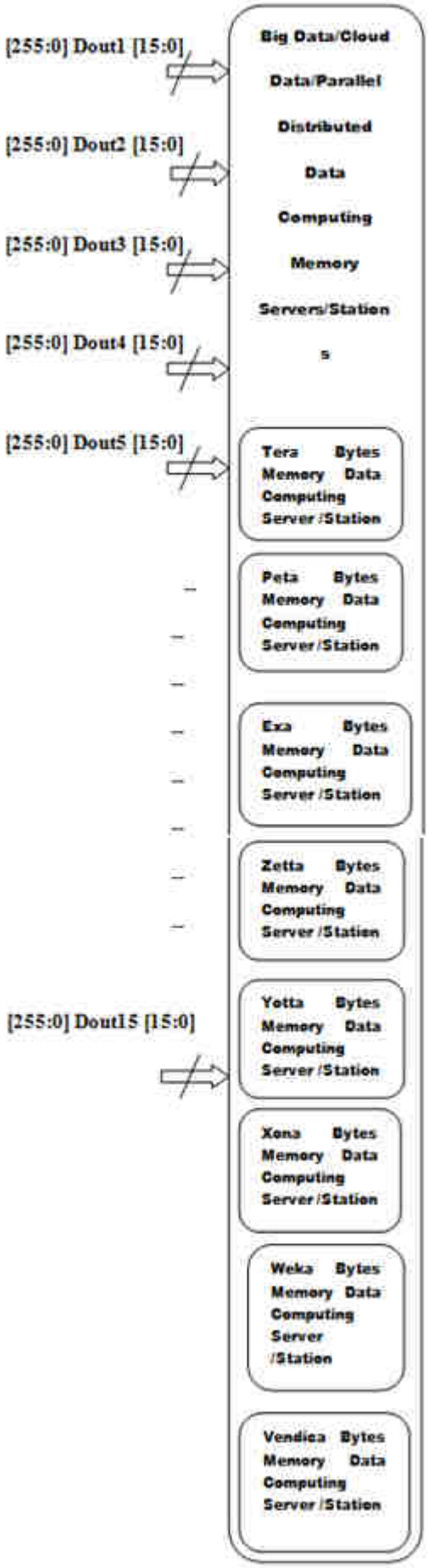
C. MULTICHANNEL PRBS CODEC



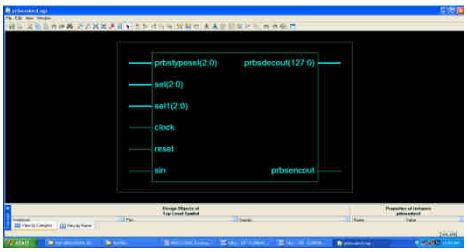


## V. Multichannel CODEC / MODEM Bus Array Design for Large /Big Data Network Computing Centers/Stations /Cloud/Internet Computing Server

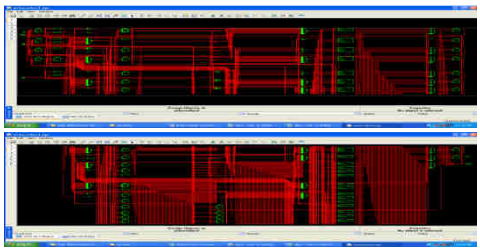




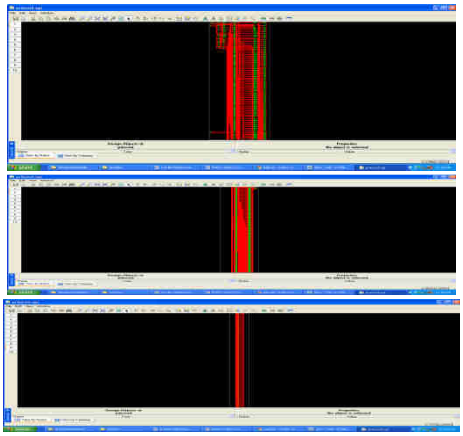

A. RTL BLOCK



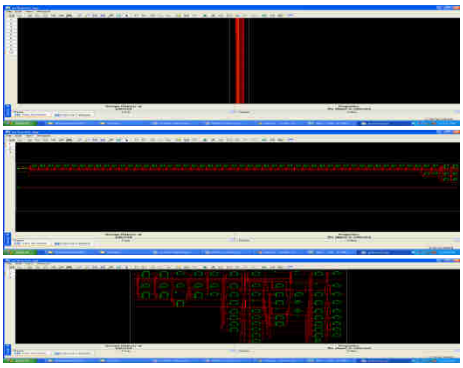

B.RTL SCHEMATIC – Multichannel PRBS CODEC



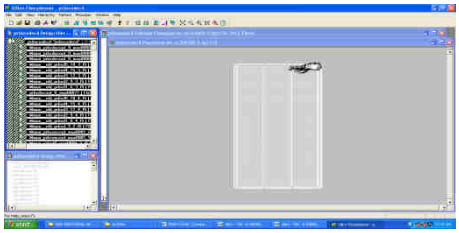
A. Multichannel Multi Clock Frequency Baud Rate (Tera Peta Exa Zetta Yotta Xona Weka Vendica Hertz Clock Frequency Synchronized ) PRBS CODEC ASIC SOC I.P Core

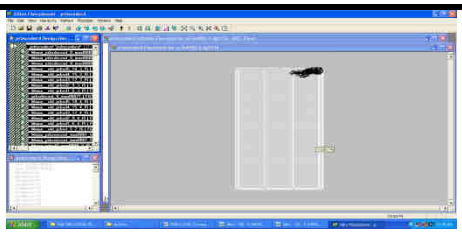


B. Technology Schematic Layout

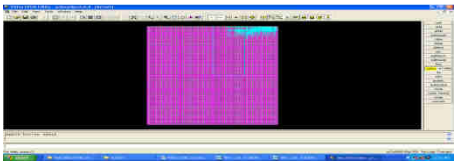


C. FPGA PLACED DESIGN REPORT

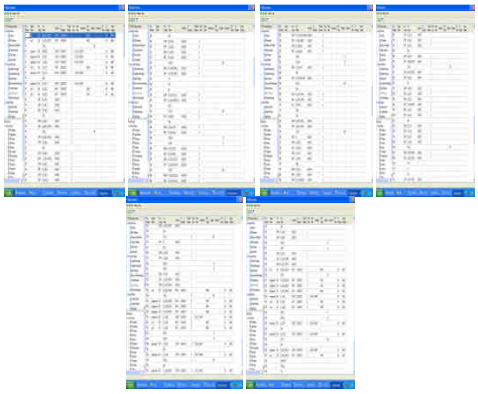




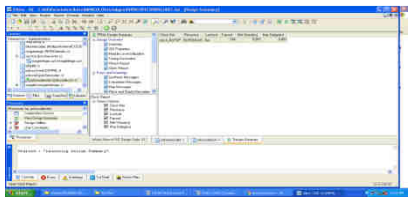
D. FPGA Routed Design Report



E. PIN OUT Report



F. CLOCK REPORT



G. ADVANCED SYNTHESIS REPORT

Final Register Report: Macro Statistics # Registers : 259 Flip-Flops : 259 # Multiplexers: 32 1-bit 8-to-1 multiplexer: 17 11-bit 8-to-1 mux: 2 16-bit 8-to-1 multiplexer: 2 24-bit 8-to-1 multiplexer:2 32-bit 8-to-1 mux : 2 48-bit 8-to-1 multiplexer: 2 52-bit 8-to-1 multiplexer: 2 64-bit 8-to-1 Mux: 2 8-bit 8-to-1 multiplexer: 1 # Xors: 16 1-bit xor2: 16# Registers: 76 Flip-Flops: 76 # Shift Registers : 12 11-bit shift register: 1 13-bit shift register: 1 18-bit shift register: 1 21-bit shift register: 4 4-bit shift register: 1 5-bit shift register: 1 6-bit shift register: 1 7-bit shift register: 1 9-bit shift register: 1

Final Report : Final Results

RTL Top Level Output File Name: prbscodecdes.ngr Top Level Output File Name: prbscodecdes

Output Format : NGC Optimization Goal : Speed Keep Hierarchy: NODesign Statistics# IOs : 141 Cell Usage : # BELS : 293 # GND : 1 # INV : 1 # LUT2 : 12 # LUT3 : 173# LUT3_L : 1 # LUT4 : 10 # MUXF5 : 63 # MUXF6 : 25 # MUXF7 : 4 # MUXF8 : 2 # VCC : 1 # FlipFlops/Latches : 181 # FDE : 21 # FDRE : 160 # Shift Registers : 16 # SRL16E: 12 # SRLC16E: 4 # Clock Buffers : 1 # BUFGP : 1 # IO Buffers : 20 # IBUF : 11 # OBUF : 9 Device utilization summary: Selected Device : 3s200tq144-5 Number of Slices: 167 out of 1920 8% Number of Slice Flip Flops:181 out of 3840 4% Number of 4 input LUTs: 213 out of 3840 5% Number used as logic: 197 Number used as Shift registers: 16 Number of IOs: 141 Number of bonded IOBs: 21 out of 97 21% Number of GCLKs: 1 out of 8 12%

Multiclock Multichannel PRBS CODEC

HDL SYNTHESIS REPORT Macro Statistics # Registers : 160 1-bit register: 88 11-bit register : 8 128-bit register: 8 16-bit register : 8 24-bit register: 8 32-bit register: 8 48-bit register: 8 52-bit register: 8 64-bit register: 8 8-bit register : 8# Multiplexer : 1 1-bit 8-to-1 multiplexer: 1 # Xors : 18 1-bit xor2 : 18Summary: inferred 3152 D-type flip-flop(s). inferred 1 Multiplexer(s). Total REAL time to Xst completion: 7.00 secs Total CPU time to Xst completion: 6.88 secs

Advanced HDL Synthesis Report Macro Statistics # Registers : 3136 Flip-Flops : 3136 # Multiplexers : 1 1-bit 8-to-1 multiplexer: 1# Xors : 18 1-bit xor2 : 18

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