International Journal of Advanced Engineering Research and Science (IJAERS) *[Vol-3, Issue-9, Sept- 2016]*
https://dx.doi.org/10.22161/ijaers *ISSN: 2349-6495(P) | 2456-1908(O)*

Analysis of Phenomenon at Quantum Capacitance Limit of SNWFET using FETToy

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Abstract— *In The proposed paper several interesting phenomenon that happens at Quantum Conductance Limit (QCL) like transconductance of One Dimensional-Silicon Nano Wire Field Effect Transistor (1D-SNWFET), mobile electron density and injection velocity is studied and simulated using Fettoy simulation tool. The selected gate material in silicon nanowire field effect transistor is SiO_2 with K=3.9 and HFO_2 with K=20. A coaxial SNWFET is simulated and the results illustrate the essential physics and peculiarities of 1D nanowire FETs, such as the saturation of channel conductance at full degenerate limit and the saturation of transconductance at the quantum capacitance limit and the full degenerate limit.*

Keywords— SNWFET, Quantum Capacitance, Non-degenerate, Full-degenerate, SiO_2, HFO_2, FETToy.

I. INTRODUCTION

A nanowire is a nanostructure with diameter of the order of a nanometer (10^{-9} meter). Alternatively nanowire can be defined as structures that have a thickness or diameter constrained to tens of nanometer or less and an unconstrained length. Typically, nanowires exhibits aspect ratio (length to width ratio) of 1000 or more. As such they are often referred to as one dimensional material and have many interesting properties that are not seen in bulk or 3D materials. This is because electrons in nanowire are quantum contained laterally and thus occupy energy levels that are different from traditionally continuum of energy levels or band found in bulk material[1]. Many different type of nanowires exist some of them are:

(a) Metallic (Ni, Pt, An)
(b) Insulating (SiO_2, TiO_2)
(c) Semiconducting (Si, In, GaN) [2]

In this paper our interest is to simulate SNWFET with different device parameters and to look its peculiar nature.

II. QUANTUM CAPACITANCE

The mobile charge Q_{TOP} depends on the potential at the top of the barrier U_{SCF}. To describe this relation a non-linear quantum or semiconductor capacitance [3-6] can be defined as:

$$C_Q \equiv \left| \frac{\partial Q_{Top}}{\partial U_{SCF}} \right| \quad (1)$$

Under high drain bias:

$$Q_{TOP} = -qn^{+} = (-qN_{1D}/2)\Im_{-1/2}(\eta_F) \quad (2)$$

So

$$C_Q = \left| \frac{\partial Q_{Top}}{\partial U_{SCF}} \right| = \left| \frac{\partial Q_{Top}}{\partial \quad _F} \frac{\partial \quad _F}{\partial U_{SCF}} \right|$$

$$= \frac{q^2 N_{1D}}{2K_B T} \frac{\partial \Im_{-\frac{1}{2}}(\quad _F)}{\partial \quad _F}$$

According to the properties of the Fermi integral, the quantum capacitance C_Q is obtained as:

$$C_Q = \frac{q^2 N_{1D}}{2K_B T} \frac{\partial exp(\quad _F)}{\partial \quad _F} = M \sqrt{\frac{q^4 m^*}{2\Pi\hbar^2 K_B T}} \exp(\quad _F) \quad (3)$$

Equation (3) is for Non-degenerate case.

$$C_Q = \frac{q^2 N_{1D}}{2K_B T \Gamma(3/2)} \frac{\partial \quad _F^{1/2}}{\partial \quad _F} = M \sqrt{\frac{2q^4 m_x^*}{\pi^2 \hbar^2 K_B T}} \quad _F^{1/2}$$

$$= M \sqrt{\frac{2q^4 m_x^*}{\Pi^2 \hbar^2 [\mu_s - (\varepsilon(0) - qU_{SCF})]}} \quad (4)$$

Above equation (4) is for full generate case, It is implied from equation (3) and (4) that the quantum capacitance increased with the gate voltage under low gate bias (Non-degenerate) while it decreases with the gate voltage under high gate bias (full degenerate). This effect is clearly illustrated in fig 1, i.e. C_Q vs. V_{GS} plots for simulated SNWFET with (a) SiO_2 layer and (b) HFO_2 layer. When the gate insulator capacitance is significantly larger than the quantum capacitance ($C_Q/C_G \rightarrow 0$), the FET works at the

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Quantum Capacitance Limit (QCL)- The potential at the top of the barrier is insensitive to the local electron charge, $Q_{TOP,}$ and is solely determined by the applied voltage biases V_G,V_D and V_S. From fig 1 it is found that $C_G < C_Q$ when $V_{GS} > 0.28V$ so the QCL is not achieved at the ON state for the SiO_2 layer [7-12].

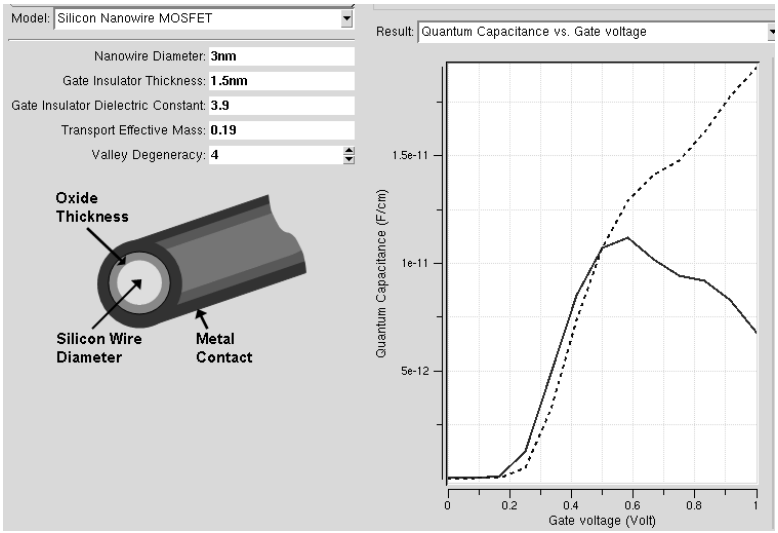

Fig.1(a): C_Q vs. V_{GS} plots for the simulated SNWT with a SiO_2 layer (k=3.9).

Table 1(a): SIMULATED OUTPUT DATA FOR QUANTUM CAPACITANCE VS.GATE VOLTAGE

Drain voltage = 1 (V)

Gate voltage (Volt), Quantum Capacitance (F/cm)

0, 4.14e-16
0.0833333333333, 7.03e-15
0.166666666667, 1.16e-13
0.25, 1.28e-12
0.333333333333, 4.9e-12
0.416666666667, 8.5e-12
0.5, 1.07e-11
0.583333333333, 1.12e-11
0.666666666667, 1.02e-11
0.75, 9.44e-12
0.833333333333, 9.2e-12
0.916666666667, 8.29e-12
1, 6.78e-12

Drain voltage = 0.0833333333333 (V)

Gate voltage (Volt), Quantum Capacitance (F/cm)

0, 1.25e-16
0.0833333333333, 2.12e-15
0.166666666667, 3.57e-14
0.25, 5.18e-13
0.333333333333, 3.22e-12

0.416666666667, 7.36e-12
0.5, 1.07e-11
0.583333333333, 1.29e-11
0.666666666667, 1.41e-11
0.75, 1.48e-11
0.833333333333, 1.61e-11
0.916666666667, 1.78e-11
1, 1.91e-11

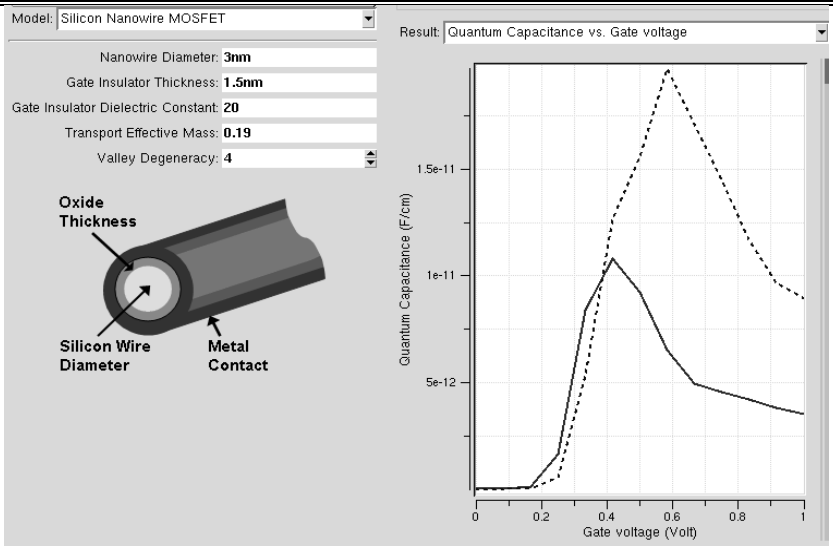

Fig.1(b): C_Q vs. V_{GS} plots for the simulated SNWT with HFO_2 layer (K =20)

Table 1(b): SIMULATED OUTPUT DATA FOR QUANTUM CAPACITANCE VS. GATE VOLTAGE (K = 20)

Drain voltage = 1 (V)

Gate voltage (Volt), Quantum Capacitance (F/cm)
0, 4.14e-16
0.0833333333333, 7.04e-15
0.166666666667, 1.19e-13
0.25, 1.66e-12
0.333333333333, 8.41e-12
0.416666666667, 1.08e-11
0.5, 9.24e-12
0.583333333333, 6.52e-12
0.666666666667, 4.94e-12
0.75, 4.57e-12
0.833333333333, 4.2e-12
0.916666666667, 3.83e-12
1, 3.53e-12

Drain voltage = 0.0833333333333 (V)

Gate voltage (Volt), Quantum Capacitance (F/cm)

0, 1.25e-16
0.0833333333333, 2.12e-15
0.166666666667, 3.6e-14
0.25, 5.79e-13
0.333333333333, 5.32e-12
0.416666666667, 1.27e-11
0.5, 1.56e-11
0.583333333333, 1.97e-11
0.666666666667, 1.71e-11
0.75, 1.45e-11
0.833333333333, 1.17e-11
0.916666666667, 9.68e-12
1, 8.93e-12

III. TRANSCONDUCTANCE OF 1D SNWFET

There are several interesting phenomenon that happen at The QCL, like transconductance of 1D SNWFET. Transconductance g_m for FET is defined as:

$$g_m = \frac{\partial I}{\partial V_{GS}}\Big|_{U_D \gg 1} = M \frac{qK_BT}{I\hbar} \frac{\partial \Im_0(\square_F)}{\partial V_{GS}}$$
$$= M \frac{qK_BT}{I\hbar} \frac{\partial \Im_0(\square_F)}{\partial \square_F} \frac{\partial \square_F}{\partial V_{GS}}$$
$$= M \frac{q^2}{I\hbar} \frac{e^{\square_F}}{1+e^{\square_F}} \frac{\partial U_{SCF}}{\partial V_{GS}} \quad (5)$$

Thus, we can obtain expression for the transconductance of SNWFET at the QCL as:

$$g_m = M \frac{q^2}{I\hbar} \frac{e^{\square_F}}{1+e^{\square_F}} \alpha_g$$
$$= M \frac{2q^2}{h} \frac{\alpha_G}{1+e^{-\square_F}} \quad (6)$$

For full degenerate:

$$g_m = \alpha_g M \frac{2q^2}{h} \quad (7)$$

The expression for the channel conductance of a SNWFET at the full degenerate limit is:

$$g_d = M \frac{2q^2}{h} \quad (8)$$

Interestingly an analytical relation between g_m and g_d at the QCL and full degenerate limit is obtained as:

$$g_m = \alpha_G \, g_d \quad (9)$$

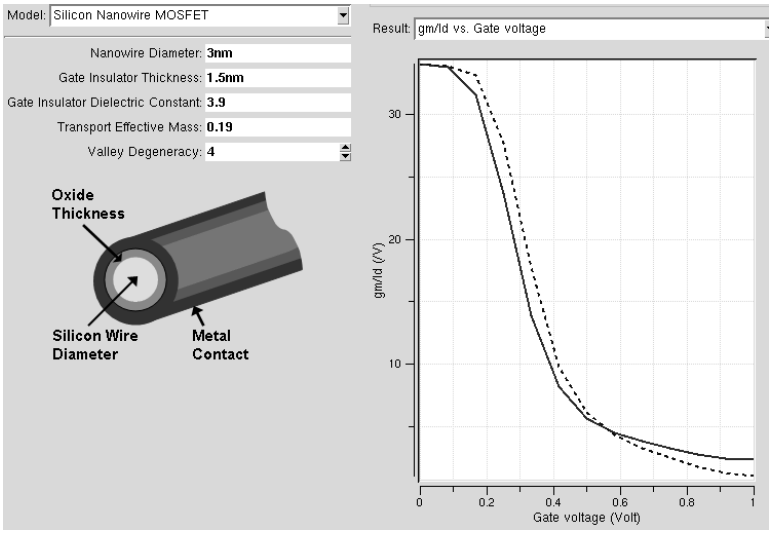

Fig.2(a): g_m vs. V_G for k = 3.9

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Table 2(a): SIMULATED OUTPUT DATA FOR g_m VS. GATE VOLTAGE (K = 3.9)

Drain voltage = 1 (V)

Gate voltage (Volt), gm/Id (/V)

0, 34
0.0833333333333, 33.8
0.166666666667, 31.6
0.25, 23.7
0.333333333333, 13.9
0.416666666667, 8.16
0.5, 5.67
0.583333333333, 4.48
0.666666666667, 3.82
0.75, 3.25
0.833333333333, 2.74
0.916666666667, 2.42
1, 2.33

Drain voltage = 0.0833333333333 (V)

Gate voltage (Volt), gm/Id (/V)

0, 34
0.0833333333333, 33.9
0.166666666667, 33.1
0.25, 27.7
0.333333333333, 17.7
0.416666666667, 9.79
0.5, 6.15
0.583333333333, 4.35
0.666666666667, 3.27
0.75, 2.47
0.833333333333, 1.81
0.916666666667, 1.29
1, 1.07

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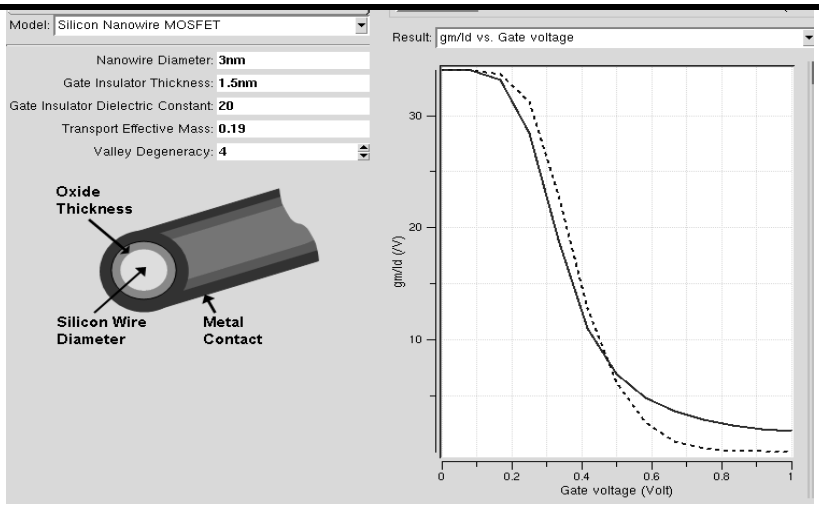

Fig.2(b): g_m vs. gate voltage for k =20

Table 2(b): SIMULATED OUTPUT DATA FOR g_m VS. GATE VOLTAGE (K=20)

Drain voltage = 1 (V)

Gate voltage (Volt), gm/Id (/V)

0, 34
0.0833333333333, 34
0.166666666667, 33.2
0.25, 28.4
0.333333333333, 18.9
0.416666666667, 11
0.5, 6.92
0.583333333333, 4.81
0.666666666667, 3.65
0.75, 2.85
0.833333333333, 2.33
0.916666666667, 1.98
1, 1.83

Drain voltage = 0.0833333333333 (V)

Gate voltage (Volt), gm/Id (/V)

0, 34
0.0833333333333, 34
0.166666666667, 33.7
0.25, 31.2
0.333333333333, 22.9
0.416666666667, 12.8
0.5, 6.16
0.583333333333, 2.56
0.666666666667, 0.897
0.75, 0.262

0.833333333333, 0.0597
0.916666666667, 0.0118
1, 0.00339

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IV. MOBILE CHARGE DENSITY OF SNWFET AT QCL

Another good way to show the features at the QCL is to plot the mobile electron density at the top of the barrier $N_{mobile} = -Q_{TOP}/q$ vs. the drain bias V_{DS}. For a conventional MOSFET, it is well known that, the gate insulator capacitance is much smaller than the semiconductor capacitance at the ON-state so N_{mobile} is controlled by the gate voltage and is independent of the drain bias if the drain induced barrier lowering (DIBL) effect is neglected. At the QCL however the potential at the top of the barrier is fixed by the applied voltage biases and the increasing drain bias vacates the – K states (n^-) while leaving the +K states (n^+) uncharged. Therefore the mobile electron density N_{mobile} at the QCL rapidly decreases from the equilibrium value as the drain bias increases from zero. When the drain bias exceeds $[\mu_s - (\varepsilon(0) - qU_{SCF})]/q$,all the –K states (n^-) have been nearly depleted so the increasing V_{DS} will not significantly reduce N_{mobile} anymore and N_{mobile} starts to saturate at a fixed value $n_{max}/2$. It should also be noted that if DIBL effect is considered, the N_{mobile} will increase with V_{DS} under high drain bias since increasing V_{DS} lowers the top of the barrier and consequently increases the degeneracy factor $\square_F$. Fig 3(a) and 3(b) plots the N_{MOBILE} vs. V_{DS} curves for the simulated SNWFET with (a) SiO_2 layer (k=3.9), (b) HFO_2 layer (k=20). The former device is working well below QCL while latter one is close to the QCL (see fig 3(a) and 3(b)). Differences between the two plots clearly illustrate the quantum capacitance effect discussed above. This effect become more and more prominent for the device characteristic of Nano scale FET as the gate capacitance continues to rise by scaling down the oxide thickness and adopting high k materials.

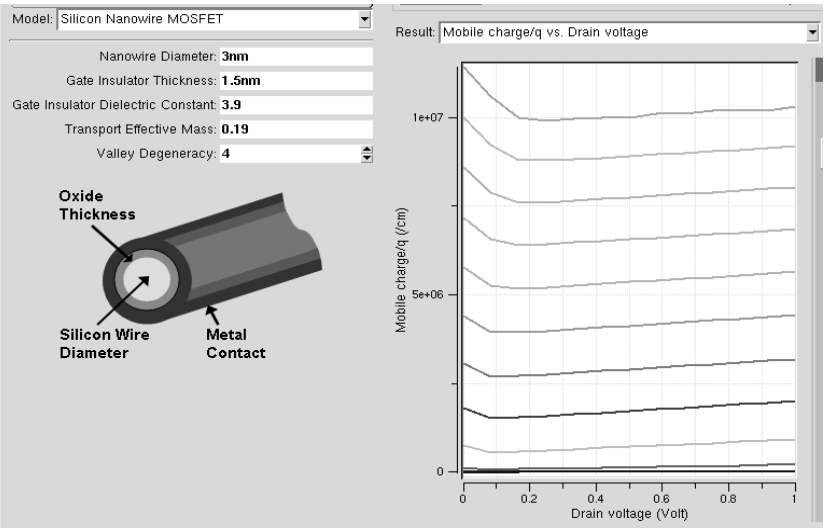

Fig.3(a): Mobile charge vs. drain voltage (k =3.9)

V. INJECTION VELOCITY

It is also interesting to explore injection velocity V_{ing} under high drain bias.
For a SNWFET V_{ing} is obtained as:

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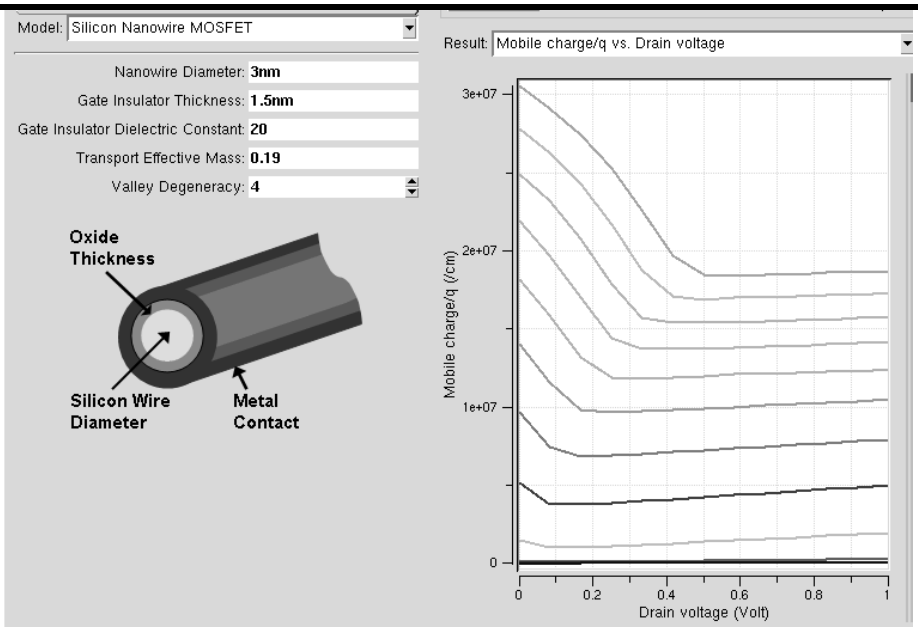

Fig.3(b): Mobile charge vs. drain voltage (k= 20)

$$V_{inj} = \frac{I^+}{q n^+} = \frac{M \frac{q K_B T}{\Pi \hbar} \Im(\square_F)}{q \frac{M}{2} \sqrt{\frac{2K_B T m_x^*}{\Pi \hbar^2}} \Im_{-\frac{1}{2}}(\square_F)} =$$

$$\sqrt{\frac{2K_B T}{\Pi m_x^*}} \frac{\Im_0(\square_F)}{\Im_{-\frac{1}{2}}(\square_F)} \qquad (10)$$

According to the properties of the Fermi integral:

$$V_{inj} = \sqrt{\frac{2K_B T}{\Pi m_x^*}} \frac{e^{\eta_F}}{e^{\square F}} =$$

$$\sqrt{\frac{2K_B T}{\Pi m_x^*}} = V_T \qquad (11)$$

Where V_T is the unidirectional thermionic velocity

$$V_{ing} = \sqrt{\frac{2K_B T}{\Pi m_x^*}} \frac{\square_F}{\lceil(2)} \frac{\lceil(3/2)}{\square_F^{1/2}} =$$

$$\frac{1}{2} \sqrt{\frac{2[\mu_s - (\varepsilon(0) + U_{Top})]}{m_x^*}} = \frac{V_F}{2} \qquad (12)$$

Where, V_F is the Fermi velocity.

Fig 4(a) shows a simulated V_{inj} vs. V_{GS} curve for SNWFET with SiO_2 layer (k=3.9) and the same curve for HFO_2 (k=20) layer is plotted in fig 4(b). It is clearly shown that under low gate bias (non degenerate) V_{inj} is equal to V_T and independent of the gate bias. Under high V_{GS} the carrier degeneracy makes V_{inj} monotonically increase with the gate bias for both k=3.9 and k=20. For k=20 when V_{GS}> 0.5 v, the device enters into full degenerate region, so, $V_{inj} = V_F/2$ and is independent of the temperature. Consequently the curves in fig 4(b) lie on the top of each other when 0.5 < V_{GS}< 1.0 V.

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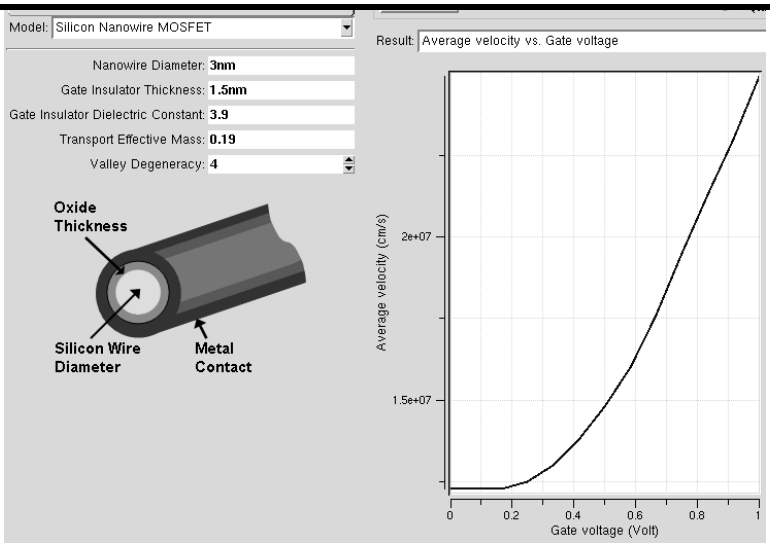

Fig.4(a): V_{inj} vs. V_{GS} for SiO_2 (k =3.9)

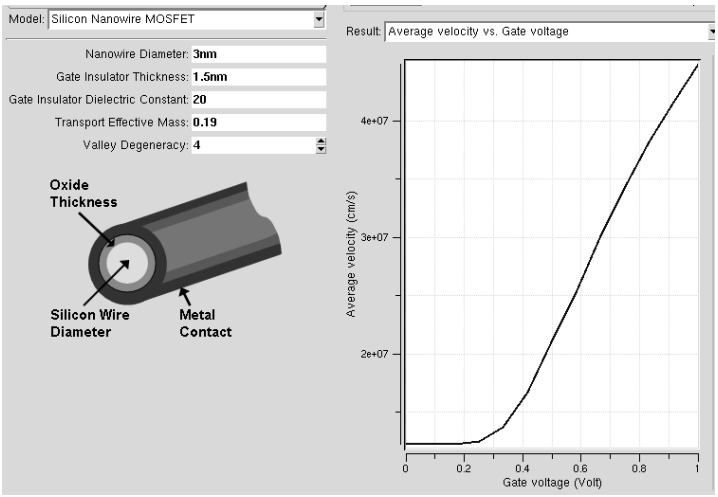

Fig.4(b): V_{inj} vs. V_{GS} for HFO_2 (k =20)

VI. CONCLUSION

In this paper we presented a simple analytical theory of various parameters of SNWFET and simulated the same using Fettoy Nano- simulator. These models were derived by modifying an analytical approach that was previously used for ballistic planer MOSFET. All the results illustrate the essential physics and peculiarities of 1D SNWFET, such as saturation of channel conductance at the full degenerate limit and the saturation of transconductance at the quantum capacitance limit as well as at the full degenerate limit.

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