Power Flow Control and Current Ripple Minimization of HVDC Converter System by Using Zero-Sequence Voltage Injection Control

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Abstract— *This paper introduces the Zero Sequence Voltage Injection(ZSVI) based Model Predictive Control (MPC) to minimize the ripples in dc current & voltage and concurrently regulate the power flow & dc current. This paper takes the benefits to calculate and inject best possible zero sequence voltage components to Parallel Hybrid Modular Multilevel Converter (PHMMC) dc bus voltage. Dc line current has been derived by discrete time dynamic model and also it expands the predictive model. Required amount of zero sequence voltage is injected to reference voltage of dc bus by using predictive model. Compared to triplen harmonic injection method, the proposed scheme improves the PHMMC performance by minimizing the ripples of dc voltage &current. Execution of the proposed methodology of PHMMC-based HVDC system is done using SIMULINK/MATLAB.*

Keywords—HVDC transmission, parallel hybrid modular multilevel converter (PHMMC), predictive control, zero-sequence voltage.

I. INTRODUCTION

The Class of modular multilevel converters (MMCs) is the most encouraging topology for the utilization of voltage-sourced converter (VSC)- based high-voltage direct-current (HVDC) transmission systems since it gives full modularity and adaptability in the design[2]. In the class of MMCs, the conventional MMC has been widely examined [2], [4]. Compared to conventional MMC, the hybrid MMCs can potentially reduces the rating of the converter components and power losses. Especially, because of less SMs working outside the main power path, a PHMMC can conceivably reduces the HVDC converter station losses in the event that it is appropriately controlled [2], [8]. This paper is centred around the control parts of a PHMMC-based HVDC station framework. One of the fundamental specialized difficulties connected with the control of a PHMMC-HVDC framework is to at the same time control the dc current/power flow and the real and reactive power. The current technique proposed to determine this issue is based on third harmonic component injection [6], [7] where a third harmonic component is injected to the reference phase voltages. Despite the fact that this strategy controls the dc bus voltage, it cannot eliminate the magnitude of the sixth-order harmonic component in the dc current. Further reduction of the dc current/voltage ripples requires injection of higher order harmonics to the dc bus voltage, which will add to the complexity in control [8]. Moreover, the triplen harmonics injection strategy has a restricted scope of ability to minimize the dc current/voltage distortions.

In this paper, a zero-sequence voltage injection (ZSVI)-based model predictive control (MPC) methodology is proposed to manage the dc current/power flow and decrease the dc current/voltage distortions of a PHMMC-HVDC framework. The MPC methodology is a promising control technique applied to power-electronic converter systems because of its fast dynamic response, adaptability to incorporate imperatives and nonlinearities of the framework, and straightforwardness in advanced usage. This paper takes the benefits of the components of the MPC procedure and adds to a discrete-time predictive model of the dc current of a PHMM HVDC station. Based on the developed model, a MPC system is proposed to: 1)control the dc current/power flow through the dc transmission line by regulating the dc bus voltage 2)minimize the dc current/voltage ripple.

II. PHMMC BASED HVDC TRANSMISSION SYSTEM

SLD of a PHMMC-HVDC network is depicted in Fig.1a HVDC arrangement contains two similar PHMMCs. One side of the PHMMC is connected to AC system through transformer and other side is connected to DC transmission line. Fig.1b shows circuit arrangement of "PHMMC-HVDC station", here ac grid connected to PHMMC unit through the transformer and also PHMMC

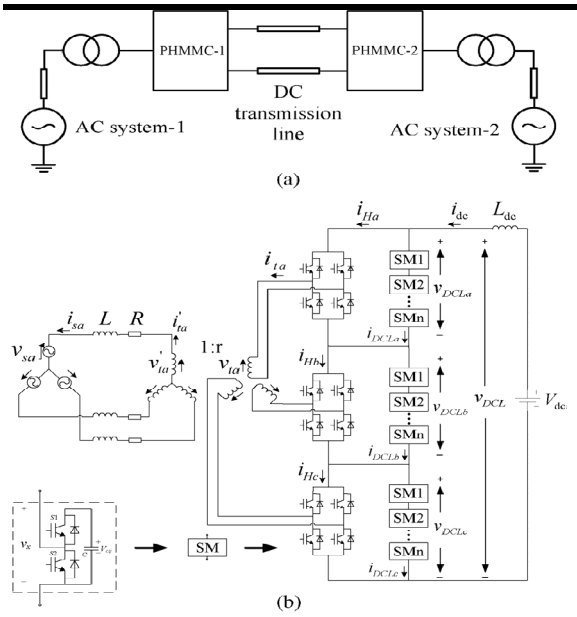

Fig. 1:Schematic representation of a PHMMC-HVDC system: (a) single-line diagram(SLD) and (b) circuit diagram of each PHMMC-HVDC converter station.

unit is connected to a dc terminal through an inductor L_{dc}at dc side. The developed regulating strategies & inferences of the paper are similarly valid for another "PHMMC-HVDC station"also[1]. All phases of PHMMC consist of full H-bridge converter & nominally identical, n number of series linked half-bridge sub modules. Fig.1b shows Sub modules of each phase and full-bridge converter are linked in parallel whereas sub modules of all the 3 $phases$ are cascaded. Thus, voltage at the dc bus is formed based on addition of the 3 $phase$cascaded sub module string voltages[1].

III. BASICS OF OPERATION OF THE PHMMC

All the SMs of PHMMC consists of a half bridge converter connected capacitor across half bridge, here the output voltage of sub module (v_x) is one or the other equal-to zero (sub module turns off or bypassed) or capacitor voltage (sub module turns on or inserted), depends on position of switch of its switch combinations, i.e, S_1&S_2. The SMs of all the phases are controlled by the switching functions, however at any time, n_j Sub modules out of $'n'$Sub modules of phase $j\ (j = a, b, c)$ are on. Where n_j is whole number in range of 0 to n & it is calculated by required AC rectified phase j voltage profile. In principle, a controllable voltage is represented by a series connected sub module string of all the phase, that is,v_{DCLj}, which is summation of inserted sub modules output voltages of phase j, as represented in Figure.1. Each phase sub module string is regulated by modulator to produce required sinusoidal rectified voltage through its terminals that is v_{DCLj}.As given in Fig.1,the voltage at the dc bus v_{DCLj} is produced by addition of individual sub module string voltages. Full bridge converter at every phase works with switching of fundamental frequency at the "zero voltage crossing" and depended on "rectified multilevel voltage waveform" produced by sub modules, produces the anticipated AC voltage of the equivalent phase[1].

Presuming that voltage of all the sub module capacitor is preferably controlled atV_{capref},an ideal $(n+1)$voltage profile of rectified waveform could produce across sub module sequences of all phases of PHMMC, v_{DCLj}. Because there exists 'n' submodules in all phases, number of included submodules, that is n_j€ {0,1,2,.....n},v_{DCLj}changes stepwise from range '0'-nV_{capref} with step size V_{capref}. Accordingly, full bridge converters working at ZVCS, v_{tj}phase voltage differs $stepwise$ in range of $nV_{capref}$to - $nV_{capref}$with V_{capref}step size and given by

$$v_{tj} = sign(v_{tjref}) n_j V_{capref} \quad \text{.....(1)}$$

$$v'_{tj} = \frac{1}{r} v_{tj} \quad \text{.....(2)}$$

And $sign(v_{tjref}) = +1, v_{tjref} \geq 0$

$sign(v_{tjref}) = -1, v_{tjref} < 0$.....(3)

where

$j = a, b, c$

v_{tj}= phase voltage at AC side

v'_{tj}=primary phase voltage of transformer

v_{tjref}= AC side reference phase voltage v_{tj}

r = ratio of transformer turns

The PHMMC AC current i_{tj} is given as :

$$i_{tj} = sign(v_{tjref}) i_{Hj} \quad \text{.....(4)}$$

$$i'_{tj} = r i_{tj} \quad \text{.....(5)}$$

Where,

i_{Hj}= phase j full bridge converter current

$i'_{tj} = i_{sj}$= transformer primary side current.

IV. ZSVI-MPC APPROACH

Here, "ZSVI-MPC" scheme is used towards controlling concurrently dc current and power flow, to reduce dc system voltage & current ripple is projected in Fig.1. In this suggested method, ZSV element is calculated &inserted into the reference voltages of 3-ϕ to control voltage of dc bus and to regulate dc current.

4.1 "Predictive-Model & Cost-Function Formulation"

The equations of mathematical model that supervise dynamic behaviour of AC voltages and are described by

$$L_{dc} \frac{di_{dc}}{dt} = V_{dc} - v_{DCL} \quad \text{.....(6)}$$

The discrete time model of the above equation deduced as

$$i_{dc}(K+1) = i_{dc}(K) + \frac{T_s}{L_{dc}}\left(V_{dc} - v_{DCL}(K)\right) \ldots\ldots(7)$$

Where

T_s= sampling period.

$i_{dc}(K)$= dc current measured.

v_{DCL} = voltage at dc bus

By presumptuous the voltages at sub module capacitor are adjusted atV_{capref},v_{DCL} is depicted by

$$v_{DCL}(K) = (N_a + N_b + N_c)V_{capref} \ldots\ldots\ldots(8)$$

Where

$N_j = n_j \pm n_z$ this represents numeral of sub modules introduced in phase j.

n_j is calculated by voltage of reference phase$V_{DCLjref}(v_{tjref})$thoughn_z is find out by the quantity of ZSV injected components, it will cancelled at transformer primary area and also do not deform the phase voltages of ac-side$V_{tj}^{'}$.

Within every sampling period, proposed MPC scheme calculate preeminent value for $V_{DCL}(N_{abc})$ which marks in lowest ripple of dc amplitude current.

To choose best V_{DCL} for manage the dc current i_{dc}, the cost function related to error of dc current can described as

$$J = i_{dc}(K+1) - I_{dcref} \ldots\ldots\ldots(9)$$

where

$i_{dc}(K+1)$ =dc current prediction of forward one-step.

I_{dcref} =dc current reference value.

By estimating the described cost function to each feasible zero sequence components, the finest possible number of sub modules are included, which lessens J& subsequently, error of dc current is chooses.

4.2 ZSVI Algorithm

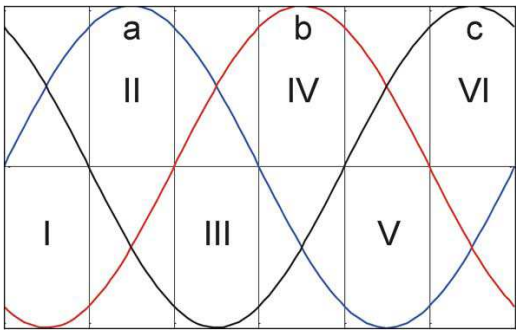

Fig. 2:One cycle with six sections.

As represented in Fig.2, line of each cycle is separated into 6 equal sections or intervals of $\pi/3$. Inside each interval, converter terminal voltage sign does not alter. From the following algorithm, $n_z$is determined:

a. In the I Section of Fig 2, by the equivalent full-bridge-converters sub module strings of ϕ a and c are switched +vely, as the sub module string of ϕ b is switched -vely. If $n_z$sub modules are summed to$n_a$and $n_c$sub module string of phase 'a' and 'c', the subsequent voltage signs of $n_z$sub modules at transformer secondary terminal are +ve. If $n_z$sub modules are summed to the $n_b$sub module string of phase 'b', subsequent voltage sign is differenced as phase b sub module string is switched -vely. Accordingly, do not make sure that ZSC are superimposed at the 3ϕ of transformer secondary terminal. Hence, if $n_b$sub modules are subtracted by n_z sub modulestring of the phase b, identical signs of the ZSC are superimposed to 3ϕ voltages at the transformer secondary terminal. In this section, to make sure N_{abc} in the value a mid 0 and n, if $N_{DCL} > (n_a + n_b + n_c)$, the minimum value of n_z is zero (i.e., $n_{zmin} = 0$) and the maximum available value of $n_z$is $n_{zmax} = \min\left(\left(n - max(n_a, n_c)\right), n_b\right)$. If $N_{DCL} < (n_a + n_b + n_c)$ then

$n_{zmin} = -\min\left(min(n_a, n_c)), n - n_b\right)$and n_{zmax}=0.

In Fig. 2 same procedures are valid for both the Sections III & V.

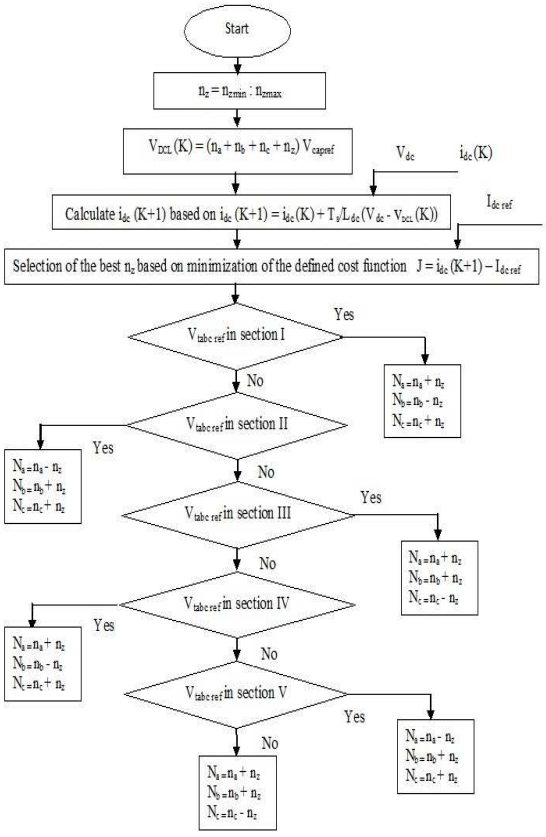

Fig.3:Flowchart of the projected ZSVI MPC scheme.

b. In II Section of Fig.2, the sub module strings of phase b & c are switched negatively with their respective full-bridge-converters, as the sub module string of phase a is switched +vely. If $n_z$sub

modules are summed to n_b&n_c SMs of phase b and c, thesubsequent voltage sign of $n_z$sub modules at transformer secondary terminal are -ve. If $n_z$sub modules are differenced by the n_a sub module string of phase a, that is switched +vely. The identical signs of the ZSC are superimposed to 3ϕ voltages at the transformer secondary terminal. In this example, to ensure N_{abc} in the value a mid 0 &n. If $N_{DCL} > (n_a + n_b + n_c)$ then $n_{zmin} = 0$ and $n_{zmax} = \min\left(\left(n - max\left(n_{b,}n_c\right)\right), n_a\right)$.If $N_{DCL}(n_a + n_b + n_c)$, then $n_{zmin} = -\min\left(min\left(n_{b,}n_c\right)\right), n - n_a\right)$ and$n_{zmax} = 0$. Same procedures are used for sections IV and VI of Fig.2.

Accurately designed for PHMMC structure & to regulate the possible numeral of ZSVC, a constraint parameter n_{zlmt} is detailed. If $n_{zmax} - n_{zmin} > n_{zlmt}$, after that$n_{zmax} = n_{zmin} + n_{zlmt}$. For illustration, if $n_{zlmt} = 1$, only there are two possible ZSVC, which is $n_z = n_{zmin}$, &$n_z = n_{zmin} + 1$, are estimated. In the mentioned technique, the behaviour of accurately planned PHMMC arrangement & by regulatingn_{zlmt}, computational burden could be controlled.

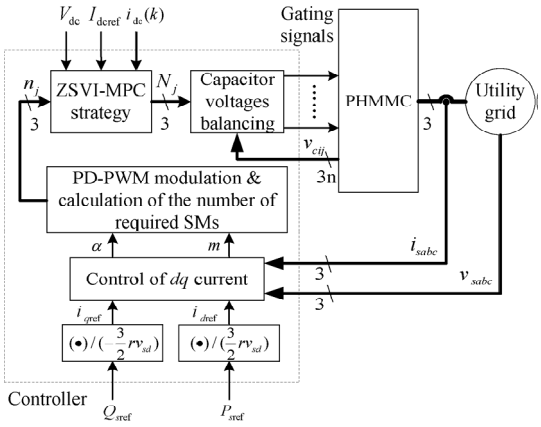

Fig. 4:Block diagram of the overall control of the PHMMC of Fig. 1.

The process outlined in Fig. 4 determines the best to track the dc current reference and to minimize the magnitude of its ripple.

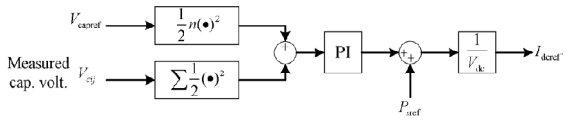

Fig.5:Block diagram of generating the dc current reference.

V. CONTROL OF A PHMMC-BASED HVDC STATION

To control the ac-side real/reactive power, a dq-current control strategy is applied to generate the reference phase voltages $v_{tabcref}$. The adopted pulsewidth-modulation (PWM) strategy to generate the voltage levels and to determine n_{abc} of the PHMMC is based on phase-disposition (PD) sinusoidal pulsewidth modulation (SPMW). To ensure the capacitor voltages of the SMs are balanced at their reference values V_{capref}, a capacitor voltage balancing technique based on a sorting algorithm is adopted [3]. Based on [6], I_{dcref} is generated and followed by I_{dc} , as shown in Fig.5.

The block diagram of the overall control of the PHMMC of Fig. 1(b) is summarized in Fig. 4.

VI. SIMULATION MODEL

6.1 MATLAB-Simulink modelled system

PHMMC-HVDC system consists of 3-ϕ supply system, converter transformer and transmission DC lines are considered. In this model ZSVI-MPC control is used to reduce the voltage & current ripples in the system. This modelled system is designed in MATLAB-Simulink workbench as the steps described below. To model this system, toolbox used is Sim-power system. Before start modelling the system, first insert the powergui and in model component designing powergui performs as an interface.The design of model is shown in fig.6.

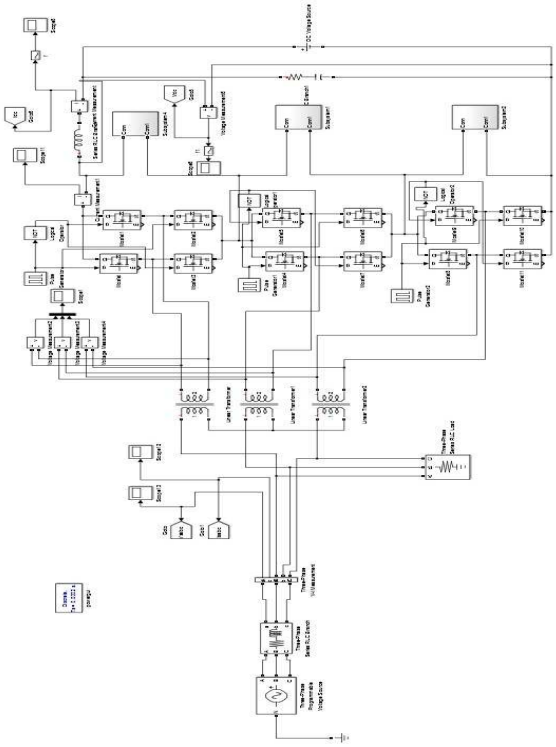

Fig.6:PHMMC-HVDC modelled system using the tool MATLAB-simulink

MPC-ZSVI has been designed in the MATLAB-simulink. The input to this system is 3-ϕ AC voltages, i.eV_a,V_b and V_c.

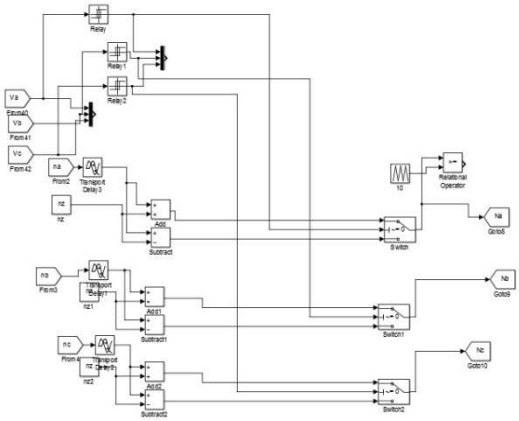

Fig.7:Design model of ZSVI-MPC in MATLAB-Simulink tool.

6.2 Simulation model of two PHMMC-HVDC systems connected to AC grid

In this section Simulation of HVDC done in MATLAB-Simulink which consists of 2 PHMMC units with identical in structure, transmission line & transformers connected to AC. It is used to simulate the system with dynamic performance.

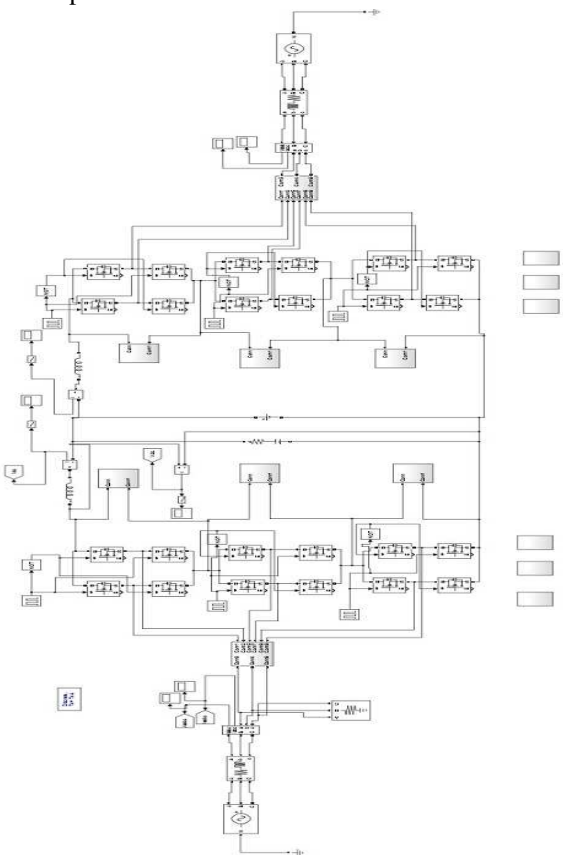

Fig.8:PHMMC-HVDC connected system model using MATLAB-simulink

VII. SIMULATION RESULTS:

Performance of PHMMC-HVDC network of Fig.1 that works with MPC scheme is described in this section. Simulation study conducted in MATLAB-Simulink workbench and exhibits the performance of control scheme in regulate the dc current & also ripple reduction. The parameters of the system are selected based on [1],[10] and are specified in the Table I.

Table 1: Study system parameters

Quantity	Value
Rated Power	20MW
Nominal Voltage of AC System (L-L)	11 KV
AC Equivalent inductance L	2.3 mH
AC Equivalent resistance R	10.37 mΩ
Nominal Frequency	50 Hz
Transformer truns ratio r	1.1
DC inductance L_{dc}	22.06 mH
Nominal net DC Voltage V_{dc}	20 KV
Sampling period T_s	200 µs
SM capacitor C	4000 µF
No. of SMS per phase n	10
Nominal SM capacitor voltage V_{cap}	1.5 KV
PWM carrier frequency	960 Hz

DC current & voltage for the projected ZSVI-MPC scheme. Current &voltage distortion magnitudes & its 6thorder harmonics are minimized with MPC control. By growing n_{zlmt}, the ripple magnitude & harmonic orders are again minimizes, when n_{zlmt}=2 and n_{zlmt} = 3..

7.1 Simulation results of PHMMC phase A steady state voltage & current and its spectrum of THD when n_{zlmt}=2

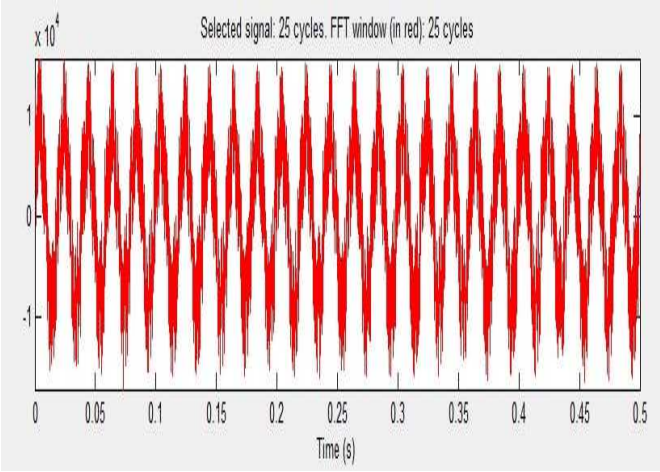

Fig 9:Steady state phase A voltage when n_{zlmt}=2

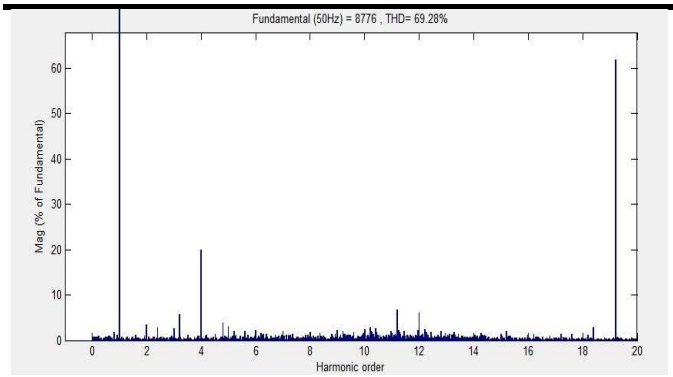

Fig.10:Spectrum of phase A voltage when n_{zlmt}=2

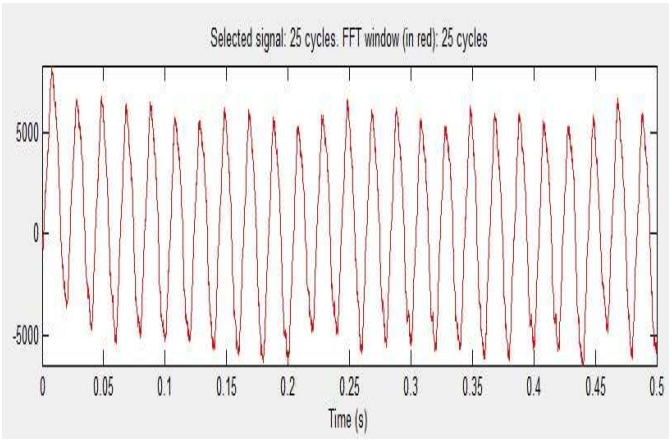

Fig. 11:Steady state ac side current when n_{zlmt}=2

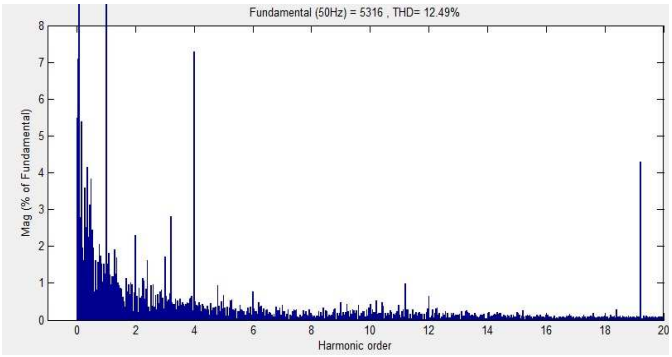

Fig.12:Spectrum of steady state ac side current when n_{zlmt}=2

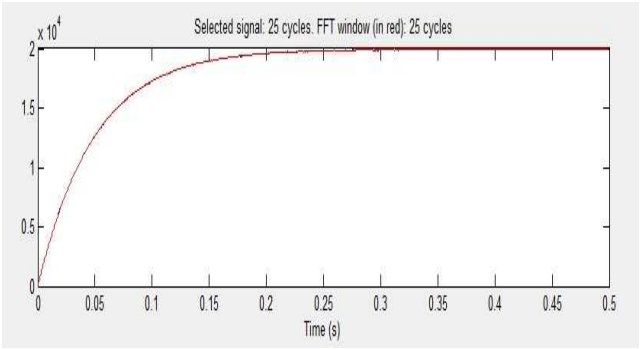

Fig.13:DC side voltage when n_{zlmt}=2

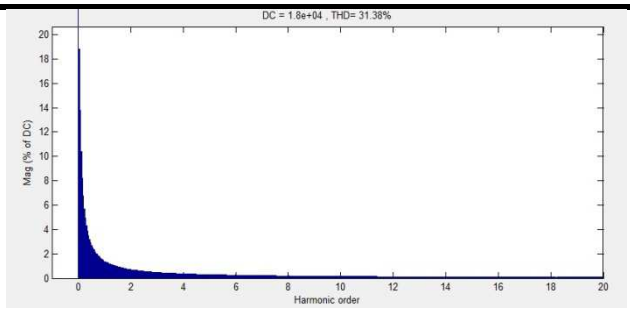

Fig 14:Spectrum of dc side voltage when n_{zlmt}=2

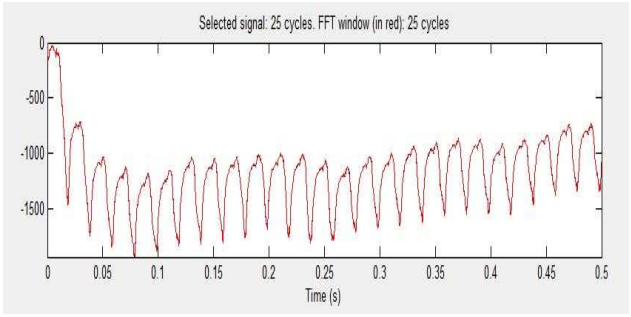

Fig.15:DC side current when n_{zlmt}=2

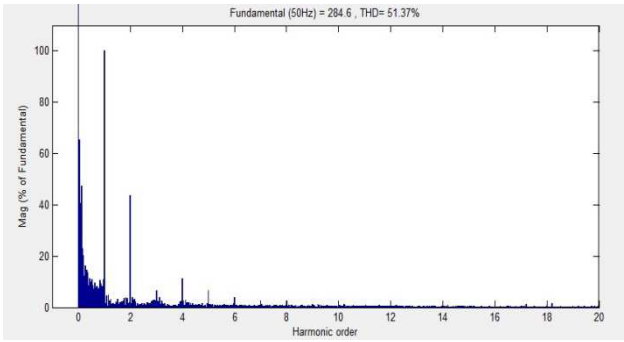

Fig.16:Spectrum of dc side current when n_{zlmt}=2

7.3 Simulation results of PHMMC phase A steady state voltage & its spectrum of THD when n_{zlmt}=3

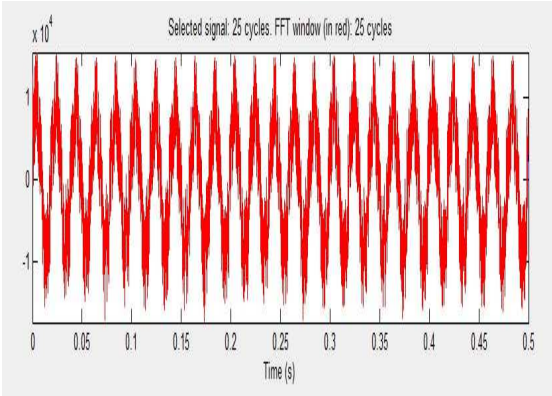

Fig.17:Steady state phase A voltage when n_{zlmt}=3

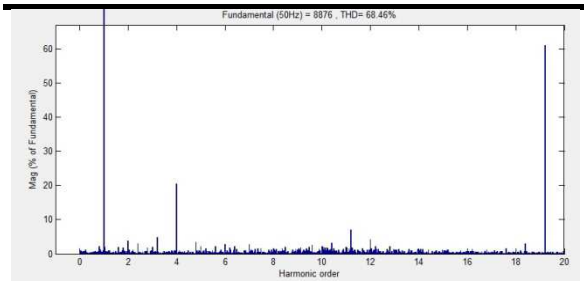

Fig.18:Spectrum of Steady state phase A voltage when $n_{zlmt}=3$

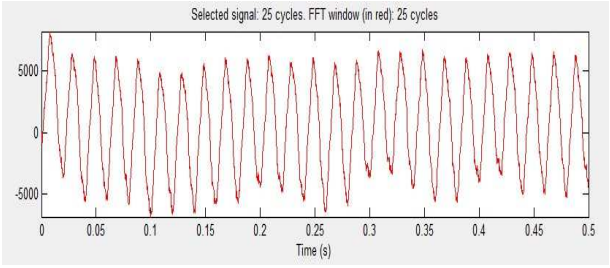

Fig 19:Steady state ac side current when $n_{zlmt}=3$

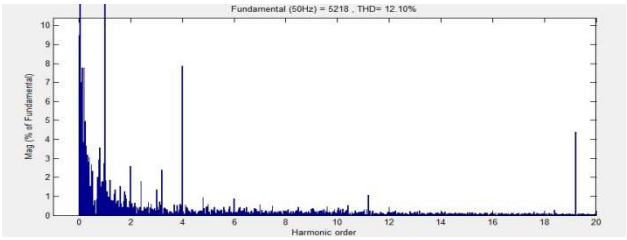

Fig.20:Spectrum of Steady state ac side current when $n_{zlmt}=3$

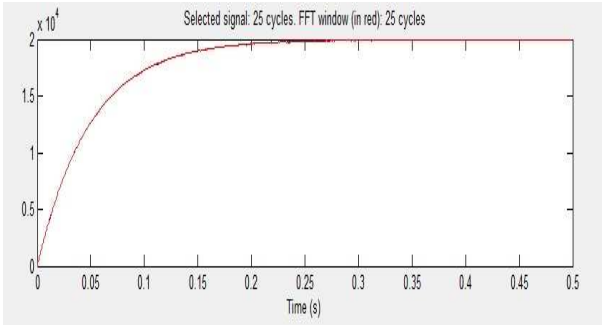

Fig.21:DC side voltage when $n_{zlmt}=3$

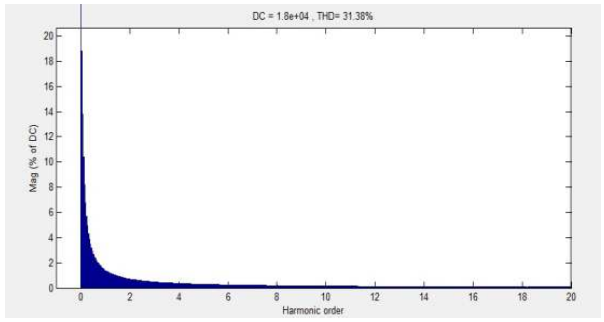

Fig.22: Spectrum of dc side voltage when $n_{zlmt}=3$

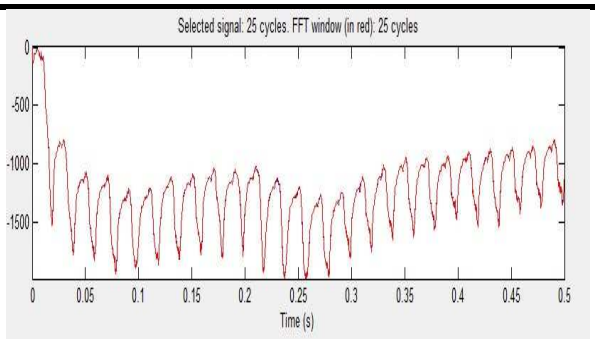

Fig.23:DC side current when $n_{zlmt}=3$

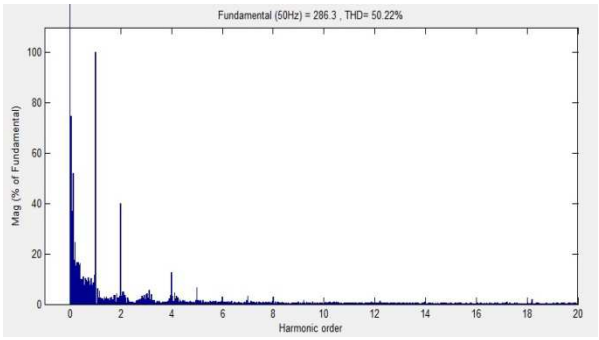

Fig.24:Spectrum of dc side current when $n_{zlmt}=3$

VIII. CONCLUSION

This paper proposes a ZSVI-MPC system to control the dc current and eliminates its ripple components for a PHMMC HVDC station. Based on the idea of predictive control, a discrete- time model of the dc current is determined. The discrete model is utilized to minimize the dc current error of the PHMMC. The viability of the proposed control technique for a 21-level PHMMC HVDC framework under different working conditions is evaluated based on simulation studies considers in SIMULINK/MATLAB. The results shows performance of the proposed control strategy in terms of the capability in regulating the dc current and power flow, and reducing ripples of dc voltage/current of PHMMC HVDC system.

REFERENCES

[1] Jiangchao Qin and Maryam Saeedifard "A Zero-Sequence Voltage Injection-Based Control Strategy for a Parallel Hybrid Modular Multilevel HVDC Converter System" in IEEE TRANSACTIONS ON POWER DELIVERY, VOL. 30, NO. 2, APRIL 2015.

[2] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for HVDC-transmission," in *Proc. IEEE Power Electronics Specialists Conf.*, Jun. 2008, pp.174–179.

[3] D. Trainer, C. Davidson, C. Oates, N. Macleod, D. Critchley, and R.Crookes, "A new hybrid voltage-

sourced converter for HVDC powertransmission," in *CIGRE Session*, 2010.

[4] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2903–2912, Oct. 2010.

[5] M. Merlin, T. Green, P. Mitcheson, D. Trainer, D. Critchley, and R. Crookes, "A new hybrid multi-level voltage-source converter with DC fault blocking capability," in *IET 9th International Conference on AC and DC Power Transmission*, London, 2010.

[6] C. Davidson and D. Trainer, "Innovative concepts for hybrid multilevel converters for HVDC power transmission," in *Proc. 9th IET Int. Conf. AC DC Power Transm. ACDC.* , 2010, pp. 1–5

[7] R. Feldman, M. Tomasini, J. Clare, P. Wheeler, D. Trainer, and R. Whitehouse, "A hybrid voltage source converter arrangement for HVDC power transmission and reactive power compensation," presented at the IET-PEMD, Brighton, U.K., Apr. 19–21, 2010.

[8] R. Feldman, M. Tomasini, J. Clare, P. Wheeler, D. Trainer, and R. Whitehouse, "A low loss modular multilevel voltage source converter for HVDC power transmission and reactive power compensation," presented at the IET-ACDC, London, U.K., Oct. 20–21, 2010.

[9] M. Tomasini, R. Feldman, J. Clare, P. Wheeler, D. Trainer, and R.Whitehouse, "DC-link voltage ripple minimization in a modular multilevel voltage source converter for HVDC power transmission," presented at the Eur. Conf. Power Electron. Appl., Birmingham, U.K., 2011.