Implementation of Status Update Module through Ethernet on Nios FPGA Platform

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Abstract—*This paper tells about the legacy devices(outdating) monitoring methodology, a simple device is designed to connect with the devices. A run time counter to check the working time of device for a monitor (equipper) and a Ethernet module for the monitoring of device from the remote station. An interconnection is established using a TCP/IP stack protocol through Ethernet connection between the hardware and the monitoring workplace. Relative data update will be sent from the hardware to the server through the form of data packets from the network. Prior data can be fed into the device so that time management and working hours of a device is known. Some devices need to work for continuously together for years so system runtime needs to be time dependent. The legacy devices are almost working in the security systems so, this device model provides a useful for monitoring purpose.*

Keywords—FPGA, Nios core, character LCD, time counter, Ethernet, ARP,TCP stack.

I. INTRODUCTION

In the present era, An embedded designs are growing faster and the use of devices is increasing enormously. Upcoming devices are being equipped with the IoT as well as the sensors included within the device itself. A new system will always be a super starter for a time being. When it gets outdated then a scope of work gets deployed a new method for increasing the lifetime of legacy devices is implemented in the following method. A device working condition monitoring creates a concentration of maintaining it properly. Some of the devices are kept working throughout continuously, for such systems monitoring is necessary. The device model is constructed using an FPGA board for its superior performance and pace and precision. This proposed design can be miniaturized by creating a new model and with the utilize of a display, Ethernet and the high rate and exact soft core CPU. There exist different soft core processor vendors in the market like Xilinx MicroBlaze, Altera Nios etc.

An FPGA design is made easy for an embedded designer to keep his ideas at a start of a specific idea. A better approach is provided to get use of the devices which are non-operating system devices. A prior use of this device can also be used as a Iot design by using Ethernet module and the different sensors to update its design by sending data to a cloud and receiving it for status update purpose.

II. LITERATURE SERVEY

Deepak karia[1], gives an idea of web server application design for home automation. This paper shows replacing the embedded server design instead of pc based model, so that single step module can be easy to use. For better use HTTP and TCP model are taken to use the server for a home automation. Srinivas keshar[2] describes the accurate Ethernet simulation model for a Ethernet and is only hope of design structure in the internet. To make the accuracy and restructure the Ethernet does not have any quality of service. He proposed eliminating the CSMA?CD model the complexity can be reduced. To compress the distributions and the curves on efficient methods can be implemented for the result of fast Ethernet. Marcelo garcia[3] models a high reliable point to point and the half duplex protocols are designed with the demand of telnet applications. The disadvantage is that a protocol resists the rules and only 1 bit in each packet is included for data transmit acquisition. Andrey sukonor[4], This design gives a description of JTAG usage in FPGA ,with the use of jtag in FPGA design. In FPGA a low footprint model can be created for a general purpose design and communication port use a JTAG is a better. To make a design flexible and powerful for the FPGA with low usage of logic elements and slow transfer.

III. EXISTING SYSTEM

The existed system are the only devices without any kind of electronic design for monitoring purpose, unless it is tested for its use. There are different kind of devices which are working outdated, for such conditions it is difficult to predict when the device goes fault. The device doesn't contain any IP socket or a display screen to check it's working.

The non operating system designs are vast and some devices are secure purpose use. Previously person used to be maintained as a controller if the device working is must for

the location. The controller used to update the system performance to the head station.

IV. PROPOSED SYSTEM

The proposed design is to create a sub-module for legacy devices to monitor its condition. This manuscript include the plan on top of FPGA using the Quatrus ii tool. The module is to establish a connection between the Hardware board or a device to the monitoring station through a Ethernet connection. A new design devices can also make use of proposed design to make inbuilt board. The design uses an LCD and a Ethernet module port on FPGA with the power supply management using CPLD. The proposed design includes two modules like monitoring place with SNMP protocol supported based monitor and the device equipped with a Ethernet port.

V. HARDWARE AND SOFTWARE USED IN THE DESIGN

Hardware : cyclone iii board EP3C120
Software : Quatrus ii and NIOS ii IDE
FPGA and Soft core processor :-
An embedded design can be modeled using FPGA platform, A soft core processor is alike a operating system based performance where a real time design can be performance valid. A FPGA is reprogrammable on a hardware design and usually the programming is done in hardware language scripts like verilog and VHDL. In this paper to design an embedded model VHDL and embedded c languages are takes to optimize the design. A lower end FPGA uses the CPLD technique are used while the technology is improving Logic elements came into existence. Cyclone iii board have a huge amount of logic elements Approximately 120K number. The board have required amount on chip memory to build this design. An Character LCD as well as the Ethernet port are used to make design successful.
Nios ii :-

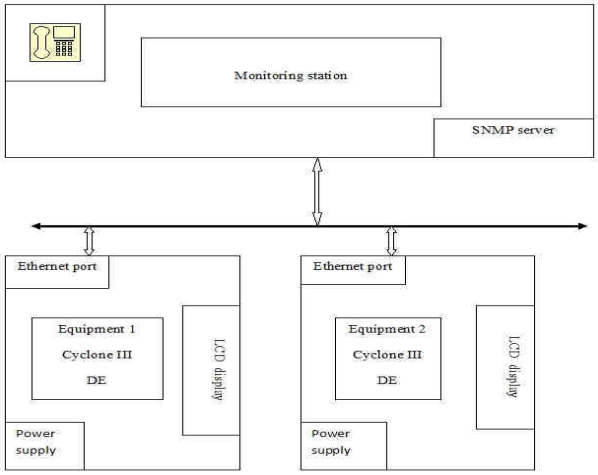

Fig.1: Proposed Model Block

The nios is a standard processor used by altera FPGA. The processor comes up with three different set of modes like NIOS/e, NIOS/s, and NIOS/f. The proposes design uses the moderate design mode to use the 9 bit embedded multiplier bit for the megawizard phase locked loop generator. Nios ii processor is RTOS based core in different set of applications can be linked together for real time design. To work with the nios ii processor a JTAG is needed to debug the application programming.

VI. IMPLIMENTATION METHODOLOGY

A Quatrus ii project uses a system generator tool to define the hardware as well as the registers in terms of functioning declarations. The system generator tool is used to generate a RTL model for the Hardware description language with the specified design.
A programmer is needed to convert the high level language to the object file using a Programmer in the tool. The functional description is developed in the nios ii software eclipse build tool to make use of a NIOS/s model of the soft core processor in the board.
The nios IDE requires the system on programmable chip information file to create an application and its board support package level model. A device driver package is created when the system generator tool is used to generate the hardware design. The model includes the LCD and the Ethernet as well as time stamp drivers from the Qsys tool.
Qsys as a system generator tool provides a minimized model for a user programmer. A convenient way of interconnecting the software and the hardware of a board design model.

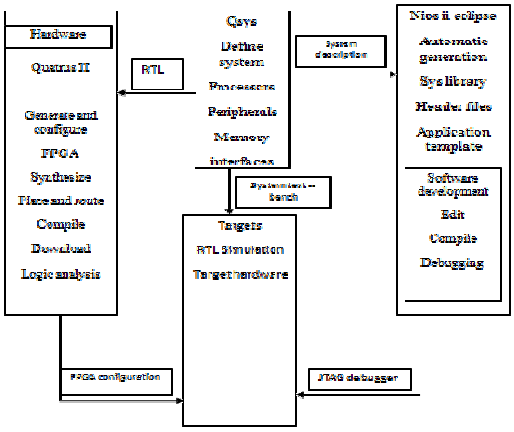

Fig.2: Implementation Flow

System generator tool specifications:-
Clock: the qsys tool works with a clock source that is generated from the board oscilator of 50MHz.
Nios ii cpu : It is connected to the clock output source and memory is allocated with the base address locations of On

chip memory and uses RISC machine as well as Nios ii moderate processor.

Onchip memory : on chip memory is used for the storing of bits and to transfer function usage. On chip memory can be set as required memory till it crocess its extent of board memory.

LCD: this paper designed model needs a character LCD screen to display the runtime of a device

JTAG UART :-Jtag is used for debugging use of functional description programming in the nios eclipse tool. In the eclipse tool every module is programmed to describe its functional design.

Interval timer : interval timer is declared to generate a timer function in the system files. It is mainly used as a system clock or a time stamp device. Any one of them can be used for the design model. Altera provide the macro declarations to use for the clock count as well as a timer counter.

PIO : This is used as a register in the programming of a device. The replica include the pio address of 8 bit length and read and write data of 32 bit as well as pio write and read select bit of standard logic.

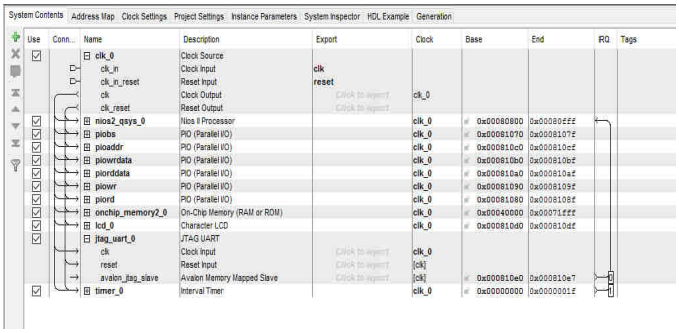

Fig.3: Qsys Structure of Proposed Work

```
component proj_new_qsys is
    port (
        clk_clk                           : in    std_logic                     := 'X';
        reset_reset_n                     : in    std_logic                     := 'X';
        piord_external_connection_export  : out   std_logic;
        piowr_external_connection_export  : out   std_logic;
        piorddata_external_connection_export : in    std_logic_vector(31 downto 0) := (others => 'X');
        piowrdata_external_connection_export : out   std_logic_vector(31 downto 0);
        pioaddr_external_connection_export   : out   std_logic_vector(31 downto 0);
        piobs_external_connection_export     : out   std_logic_vector(7 downto 0);
        lcd_0_external_data               : inout std_logic_vector(7 downto 0)  := (others => 'X');
        lcd_0_external_E                  : out   std_logic;
        lcd_0_external_RS                 : out   std_logic;
        lcd_0_external_RW                 : out   std_logic
    );
end component proj_new_qsys;

u0 : component proj_new_qsys
    port map (
        clk_clk                           => CONNECTED_TO_clk_clk,                           --
        reset_reset_n                     => CONNECTED_TO_reset_reset_n,                     --
        piord_external_connection_export  => CONNECTED_TO_piord_external_connection_export,  --
        piowr_external_connection_export  => CONNECTED_TO_piowr_external_connection_export,  --
        piorddata_external_connection_export => CONNECTED_TO_piorddata_external_connection_export, --
        piowrdata_external_connection_export => CONNECTED_TO_piowrdata_external_connection_export, --
        pioaddr_external_connection_export   => CONNECTED_TO_pioaddr_external_connection_export,   --
        piobs_external_connection_export     => CONNECTED_TO_piobs_external_connection_export,     --
```

Fig.4: Qsys Component Generator

Software application functional design :-

To develop a functionality between the hardware and software modeling a debugger is used . Nios works on C language based working. JTAG is used in the proposed model to establish a connection from hardware to software linking. An Ethernet port is used to transfer the data between monitor station and the target hardware board. A TCP/IP model is used to establish a link between the Ethernet protocol transfer from the board to working place. The protocol uses a ARP and the SNMP to send and receive the data packets. A network is created between the device models. ARP uses a message packet of address and that address size might of upper or lower value layers of OSI. The ARP protocol mainly valid on the IPv4 network mainly. The Ethernet port works in the RGM II mode and is used to vary the speed of gigabit as well as the duplex signals. With the use of 25 MHz clock the speed of transferring packets vary from 10/100 gigabit . If an oscillator of clock speed 125 MHz clock is used as a receive clock then 1000 mbps speed of gigabit data path will be selected.

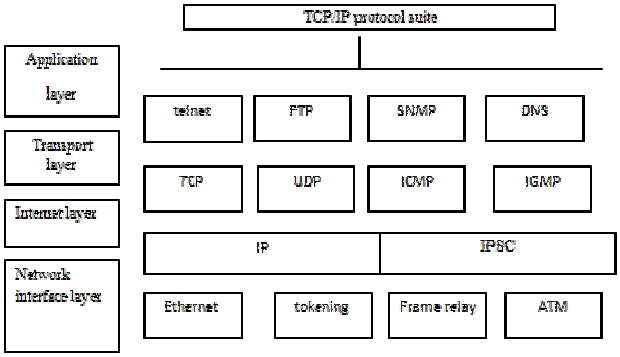

Fig.5: TCP Suite Flow

A signal tap ii analyzer is used to capture the clock signals as well as the register data transmission of data certain period of time with a exact value. The tool is mostly used by the altera FPGA. It is used to find the node value of a signal designs and the triggering modes are used to find the values of PIO read and write data values. A multiple triggering values are given for a continuous measure of clock pulses that is o either edge triggering manually.

When a signals are added from the signal ii tap analyzer there will be use of logic elements in the device. On comparing the results the number of logic elements varying can be seen and the memory allocation also changes.

The following figures are the outcomes of data transfer from the Ethernet as well as the board. With the increment of clock counter the data updating will be captured till a sample depth of 2K range.

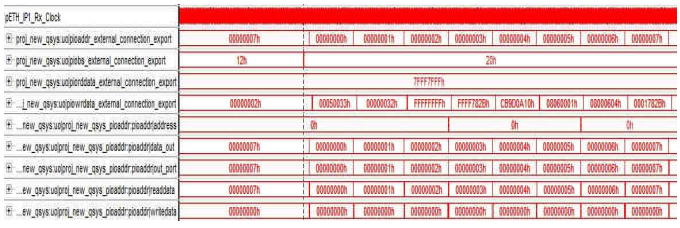

Fig.6: Export Of Device Data to the Monitor

A small counter cock is generated by using a timestamp driver in the system generation, a set time of day , get time of day and the local time macros are used to optimize the design.

Fig.7: System Working Time Counter

VII. CONCLUSION AND FUTURE WORK

Conclusion:

A device is connected to the legacy equipment and is monitored with the help of a Ethernet connection driving between the monitor station (SNMP server) and the hardware board.

Future work:-

The Device model can be interfaced with the sensors to capture the environmental conditions as well as the design can be optimized to build a safe and minute base issue model.

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