Jurnal Sains Materi Indonesia
Indonesian Journal of Materials Science

Vol. 11, No. 2, Februari 2010, hal : 112 - 117
ISSN : 1411-1098

Akreditasi LIPI Nomor : 536/D/2007
Tanggal 26 Juni 2007

EFFECT OF INTERDOT RESISTANCE ON SINGLE ELECTRON DEVICES WITH SILICON MULTI DOTS

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ABSTRACT

EFFECT OF INTERDOT RESISTANCE ON SINGLE ELECTRON DEVICES WITH SILICON MULTI DOTS. The effect of interdot resistance on single electron devices with Si (silicon) multi dots has been studied in this work. The devices were fabricated by a fabrication method consisting of three steps, i.e., sample preparation by wafer bonding technique, formation of Si dots and formation of Si channel and electrodes. It was found that the interdot resistance, which is influenced by the thickness of the interdot barrier region, determines the localization of the carrier. The device with strong carrier localization reveals the current oscillations on the drain current versus gate voltage characteristics. Such characteristics are caused by the Coulomb blockade effect, and this means that the device works based on single electron phenomenon. These results indicate that the interdot resistance plays an essential role on the device operation.

Key words : Single electron device, Coulomb blockade, Multi dots, Interdot resistance

ABSTRAK

RESISTANSI ANTAR *DOT* PADA DIVAIS ELEKTRON TUNGGAL DENGAN SILIKON *MULTI DOTS*. Efek resistansi antar dot pada divais elektron tunggal dengan Si (silikon) *multi dot* telah dipelajari pada penelitian ini. Divais yang digunakan dibuat melalui metoda fabrikasi yang terdiri dari tiga proses, yaitu preparasi sampel dengan *wafer bonding*, pembuatan Si *multi dot* dan pembuatan kanal Si dan elektroda. Ditemukan bahwa resistansi antar *dot* yang dipengaruhi oleh ketebalan bagian penghubung antar *dot*, menentukan terlokasinya muatan listrik atau tidak. Divais dengan lokalisasi muatan yang kuat, menghasilkan osilasi arus listrik pada karakteristik arus *drain* terhadap tegangan *gate*. Karakteristik tersebut disebabkan oleh efek *Coulomb blockade* , dan ini berarti divais bekerja atas dasar fenomena elektron tunggal. Hasil ini mengindikasikan bahwa resistansi antar *dot* memegang peranan yang esensial pada operasi divais.

Kata kunci : Divais elektron tunggal, *Coulomb blockade*, *multi dot*, Resistansi antar *dot*

INTRODUCTION

Single electron devices [1] based on the Coulomb blockade and quantum size effect, such as single electron transistor (SET) [1,2] or single electron memory [3] are expected to be key devices for future extremely large-scale integrated circuits (LSIs) because of its ultra low power consumption and small size. In order to realize such devices working at high temperatures near room temperature, it is necessary to make the devices with the size of less than 15 nm. Moreover, it is also essential to fabricate the devices using Si (silicon), because they will be compatible with conventional LSIs process technology. For this purpose, various novel approaches have been demonstrated, such as pattern-dependent oxidation [2,4] scanning tunneling microscope nano-oxidation process [5] anisotropic wet etching [6] and so forth.

Recently, the development of silicon-on-insulator (SOI) technology provides a uniform single-crystalline Si layer, which enables us to fabricate Si quantum slabs [7] wires [8,9] and dots [2,10]. Takahashi *et al.* [2] investigated the device operation of Si SET devices with one single-crystalline dot coupled with twotunnel capacitors, using separation-by-implanted-oxygen (SIMOX) substrates [11] which is one of the SOIs. They measured the source-drain conductance and observed, in source-drain current versus gate voltage curves, conductance oscillations (or Coulomb oscillations) at room temperature due to the Coulomb blockade, an effect

in the single electron phenomena. Another type of SOI devices is SET device with Si multi dots channel, as reported by Uchida *et. al.*[9] and Ratno *et al.* [12,13]. The Coulomb blockade oscillations under 80 K were also observed in this device. However, even the SET device with Si multi dots has been reported by several groups, the phenomena have not been well understood, especially the interaction between the dots. In this device, the interdot Si region between neighboring dots works as the potential barrier (or tunneling junction) due to a quantum effect and plays an essential role in the device operation.

The purpose of this work is to fabricate and study Si SET devices with multi dots focusing on thickness effect of the interdot barrier region. In this work, SET devices with Si multi dots were fabricated in ultrathin SOI materials. The Si multi dots are fabricated by a nanometer-scale local oxidation of Si (nano-LOCOS) process,14 which enables us to control the dot size as well as tunnel resistance between Si dots.

EXPERIMENTAL METHOD

Device Structure

The structure of the device is schematically shown in Figure 1. The device structure is almost the same as that of a metal-oxide-semiconductor field-effect transistor (MOSFET) fabricated in an SOI substrate, but the device has two key features, i.e., the Si multi dots are fabricated in the patterned Si (p-type (100), 14Ωcm) channel and the base Si substrate works as a back gate. The width and length of the Si channel are designed to be 0.2μm and 0.8μm, respectively.

Fabrication Method

To fabricate devices in Figure 1, we employed a fabrication method, consisting of three steps, i.e., sample preparation by wafer bonding technique, formation of Si dots and formation of Si channel and electrodes. Such fabrication sequence is designed in order to avoid the agglomeration phenomena of a thin Si layer. This is because of the agglomeration becomes an obstacle for device fabrication. It will be shown that an ultrathin (<20 nm) Si layer is used for formation of the device.

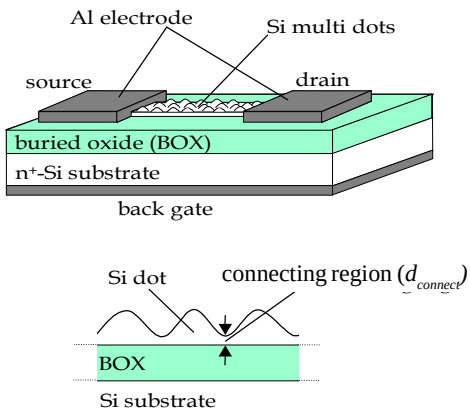

Figure 1(a). Schematic view of the device and (b) Cross-sectional view of Si channel

Sample Preparation by Wafer Bonding Technique

In this step, a SOI wafer used in this work was fabricated by wafer bonding technique, which consists of a (100) SOI (top Si) layer (B-doped; 14Ωcm), a 90-nm-thick buried oxide (BOX) layer and an n+-Si(100) substrate (resistivity: 0.008Ωcm). The reason for using this SOI wafer is that the fabrication method enable us to control the BOX thickness precisely, ranging from 1 nm to 100 nm. The type of the base Si substrate can be also changed by this technique. In this work, however, it is necessary to use high-doped base Si substrates because of the following reasons: (1) to utilize of the base Si substrate as a back gate electrode; (2) to control easily the sample annealing by direct current heating in the dots formation (nano-LOCOS) process. It should be noted that conventional SOI wafers have a low-doped top Si layer and a base Si substrate.

Then, the top Si layer is thinned by repetitive cycles of thermal oxidation and subsequent chemical etching to the desired thickness, i.e., 19 nm. It is noted that the initial thickness of the top Si before thinning process is about 140 nm. The top Si layer thickness, 19 nm, is thick enough to prevent the agglomeration of the SOI layer when high temperature cleaning is done in the nano-LOCOS process.

Si Multi Dots Formation by Nano-LOCOS

Figure 2 shows formation of the Si multi dots in the Si layer by the nano-LOCOS process. The process consists of three steps, i.e., formation of SiN islands by thermal nitridation, selective oxidation with the SiN masks and removal of SiN islands and SiO_2. Detail of these steps are as follows:

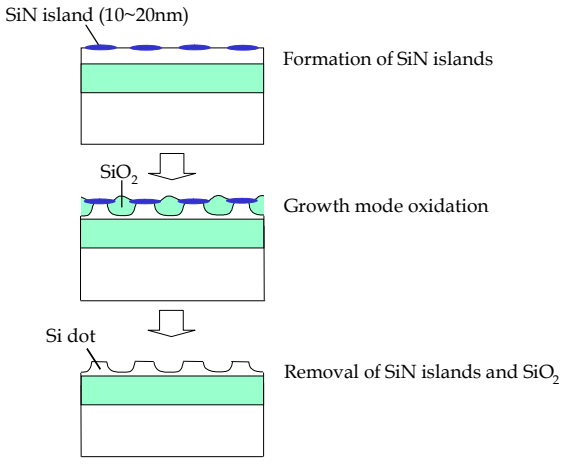

Figure 2. Steps in nano-LOCOS process

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Prior to loading into an ultrahigh vacuum (UHV) chamber, the sample is chemically cleaned by H_2SO_4/H_2O_2 and then rinsed in deionized water. (By this procedure, a 1-nm-thick chemical oxide was formed on the surface). After high temperature flash cleaning of the SOI surface in UHV at 900°C for 10 s, the Si surface is nitrided in a N_2 ambience ($1x10^{-5}$ Torr) at 750 °C for 100s to form small SiN islands naturally. It was confirmed that SiN islands with average lateral size, height and inter-island spacing (i.e., distance between neighboring island`s edges) of about 20 nm, 0.5 nm and 20 nm, respectively, are obtained.

The average lateral size and density of SiN islands depend on the nitridation temperature and time, and therefore they can be varied over a wide range, if necessary. In contrast, the height of the SiN islands (only 0.5 nm) is almost not influenced by the pressure, temperature and time when N_2 is introduced in the UHV vacuum. However, it has been confirmed that they work as oxidation masks and only bare Si region is selectively oxidized.

The next stage is the selective oxidation step. Here, we employed a conventional furnace oxidation, i.e. oxidation an O_2 atmosphere. In this oxidation condition, an SiO_2 film is grown on the Si surface. Since the SiN islands work as an oxidation mask, Si dots can be obtained by this oxidation. In this structure, the height of dots and the thickness of interdot connecting region ($d_{connect}$) depend on the oxidation condition. By controlling the oxidation conditions, two samples with different $d_{connect}$ (but almost same dot height) were prepared, *i.e.*, $d_{connect}$ =13 nm (sample A) and $d_{connect}$=5 nm (sample B). Such connecting regions work as tunnel barrier interdot. Figure 3 shows an atomic force microscope (AFM) image of fabricated Si multi dots just after removing SiO_2. The height and the density of dots are achieved to be 4 nm and $3x10^{11}cm^{-2}$, respectively.

Formation of Si Channel and Electrodes

As shown in Figure 4, the SOI layer is patterned by conventional electron-beam lithography and selective etching with a KOH solution to form Si channel

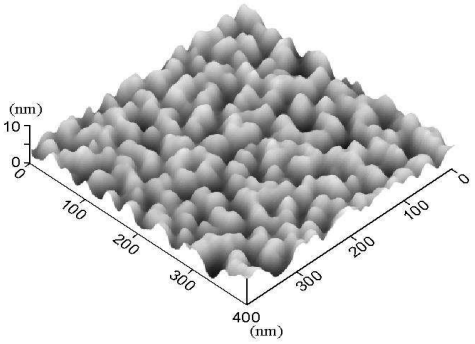

Figure 3. AFM image of Si multi dots taken after nano-LOCOS process.

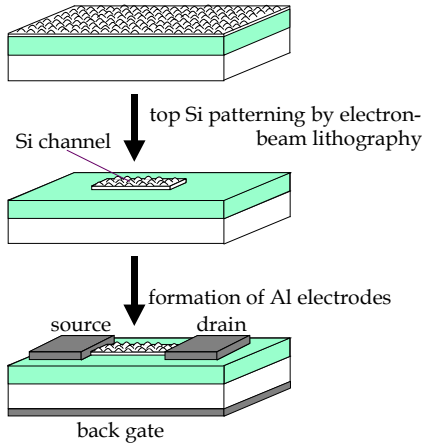

Figure 4. AFM image of Si multi dots taken after nano-LOCOS process.

with channel width of 0.2μm. Then, the device fabrication was completed by Al electrodes formation with a distance between source and drain of 0.8μm. Because one dot has 10~20 nm in diameter, the number of dots between source and drain is estimated to be about 25.

The electrical characteristics of the fabricated devices were then measured with HP4140B precision semiconductor parameter analyser. For this measurement, it is defined that the source is electrode which is connected to a ground, and the drain is one which is connected to voltage source and current meter.

RESULTS AND DISCUSSION

Figure 5 shows the drain current (I_{sd}) versus drain voltage (V_{sd}) characteristics for the devices measured at 15 K. The current of device A is much smaller than that of device B. This result indicates that the conductance of the Si channel strongly depends on the thickness of interdot connecting region ($d_{connect}$).

Figure 6 shows the schematic views of the multi dots and their corresponding potential (lowest energy level) for samples A and B. Based on quantum mechanic, height of tunnel barrier will be proportional to $[d_{connect}]^{-2}$. It can been seen that the barrier height of device A is about ten times higher than that for device B. It is noted

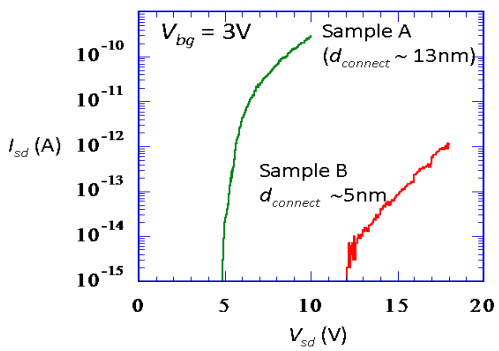

Figure 5. Drain current (I_{sd}) vs drain voltage (V_{sd}) characteristics for devices A and B at 15K.

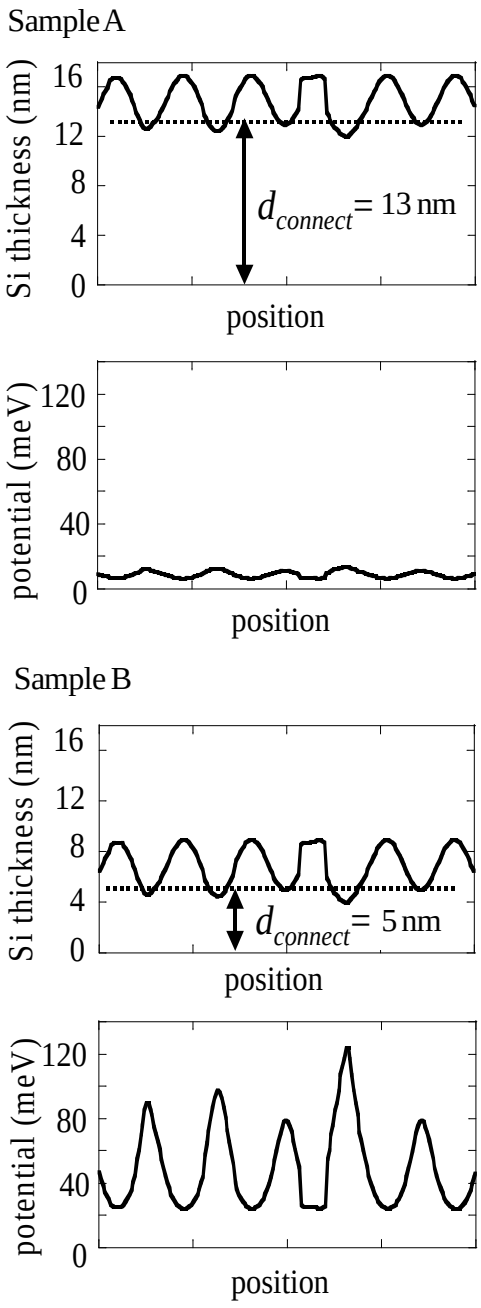

Figure 6. Schematic views of the multi dots and their corresponding potential for samples A and B.

that various barrier height and width are caused by the random sizes of the multi dots. Here, the barrier height originates from the difference of ground level in the top of dot and valley between dots. For sample A with $d_{connect}$= 13 nm and a dot height of 4 nm, the barrier height is estimated to be 5 meV and 2 meV for electron and hole, respectively. The low barrier height is formed since the dconnect is large. As a result, the tunnel resistance is smaller than the quantum resistance. In other words, the carrier (electron or hole) is weakly localized. In this condition, Coulomb blockade conditions will be difficult to be satisfied and random tunneling occurs in the barriers. For sample B, $d_{connect}$= 5 nm and a dot height of

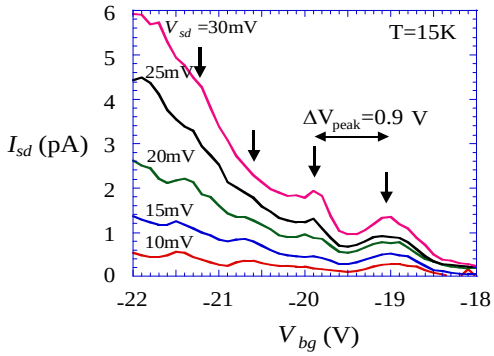

Figure 7. Drain current Isd versus gate voltage Vbg characteristics of sample B at 15K.

4 nm, the barrier height is estimated to be 55 meV and 21 meV for electron and hole, respectively. Here, $d_{connect}$ is small, so that the barrier height is high. Consequently, the tunnel resistance is larger than the quantum resistance, resulting in the strong localization of the carrier.

Figure 7 shows the drain current I_{sd} at small drain voltage V_{sd}, as a function of gate voltage V_{bg}. As shown in the figure, the current oscillations due to Coulumb blockade effect are clearly observed. The points indicated by arrows are the oscillation peaks. It has been confirmed that such oscillations are not found for device B because of weaker carrier localization in the dot due to lower tunnel barrier.

The observed period in the curves, however, is not constant. One reason might be that stochastic Coulomb blockade occurs here. It should be noted that the Coulomb oscillations for the multi-tunnel junctions are irregular (stochastic Coulomb blockade) as reported by Kemerink *et. al.* [17] This is probably due to the overlapping of the closely spaced Coulomb blockade regions one another.

Figure 8 shows I_{sd} - V_{sd} characteristics observed at 15 K. The Coulomb gap with ΔV_{gap}= 60 mV gap is observed. Moreover, the telegraphic noise in the negative V_{sd} bias are also observed, as indicated by an arrow. It is strongly suggested that a current shift occurs due to charging and discharging at dots adjacent to the current path.

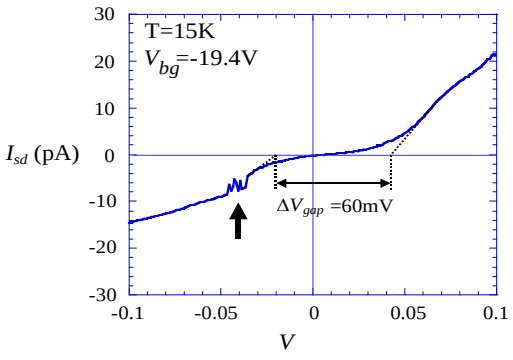

Figure 8. I_{sd} versus V_{sd} characteristics of sample B at 15 K for V_{bg}=-19.4V.

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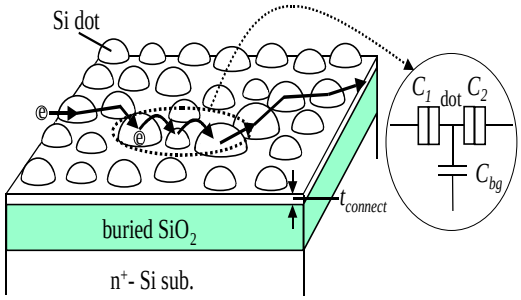

Figure 9. Single charge percolation path

It is supposed that a percolation path between source and drain is formed in the channel as shown in Figure 9. However, highest resistance tunnel junctions dominate the carrier transport and thus the Coulomb blockade oscillation (Figure 7) may be dominated by a single dot and neighboring tunnel barriers. From the observed oscillation in Figure 7, the back gate capacitance C_{bg} is discussed. A comparison can be made between the capacitance C_{bg} given by Coulomb oscillations and the estimated capacitance by considering the structural feature of the device with BOX thickness of 90 nm. From Coulomb oscillations, the C_{bg} is estimated to be 0.17 aF from $C_{bg}=e/\Delta V_{peak}$ by taking the period of 0.9 V (1 aF=10^{-18} F). For estimation of C_{bg} by considering the device structure, it is assumed that the dot shape is semi-spherical shape as shown in Figure 10. For this case, the capacitance is expressed as

$$C = \frac{\varepsilon_{SiO_2}\varepsilon_o S}{t_{BOX}} \quad \text{.....} \quad (1)$$

$$S = \pi a^2 \quad \text{.....} \quad (2)$$

where :

ε_o = Dielectric of vacuum
ε_{SiO2} = Relative dielectric constant of SiO_2
a = Radius of dot
t_{BOX} = BOX thickness

From AFM observation, the a is about 10 nm. For ε_{SiO2} = 4 , a = 10 nm and t_{BOX} = 90 nm, the C is estimated to be 0.12 aF, which is in good agreement with the calculated capacitance from Coulomb oscillations. This result strongly suggests that the observed I-V characteristics are determined by the Coulomb blockade phenomena.

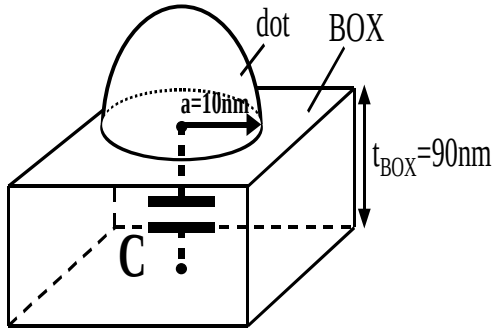

Figure 10. Semi-spherical dot shape for calculation of capacitance C_{bg}

The total capacitance of the dot is estimated from I_d-V_d characteristics in Figure 8. The total capacitance of the dot, C total, is estimated to be about 2.7 aF from C total=$e/\Delta V_{gap}$ by taking the Coulomb gap ΔV_{gap} of 60 mV. This value corresponds to charging energy (=e^2/C_{total}) of 60 meV, which is larger than the thermal energy kT at 15 K of 1.3 meV, which assures the single electron phenomena occurs.

CONCLUSIONS

We have succeeded in the fabrication of the SET devices with Si multi dots using SOI material. The fabrication method consists of three main processes, i.e., sample preparation by wafer bonding, formation of the single-crystalline Si multi dots by nano-LOCOS and formation of Si channel and electrodes. Electrical characteristics measurements show the current oscillations due to the Coulomb blockade effect. It was also found that the thickness of the interdot connecting region plays a key role in the phenomena.

ACKNOWLEDGEMENTS

The author wish to acknowledge T. Mizuno of Shizuoka University, Japan for his technical support.

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